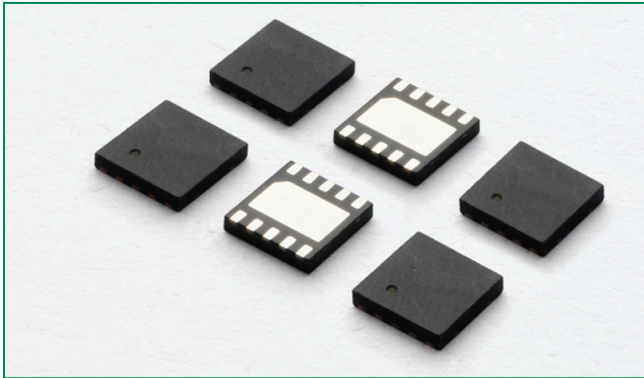
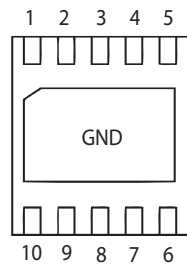


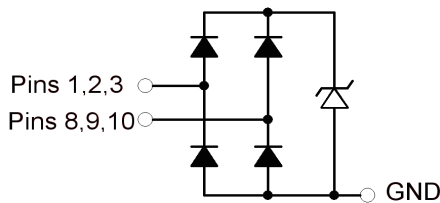
## SP4042 Series 3.3V Diode Array



### Pinout



### Functional Block Diagram



### Description

The SP4042 integrates low capacitance steering diodes with a TVS diode to provide 2 channels of protection against lightning induced surge events and ESD. This robust device can safely absorb up to 120A per IEC61000-4-5 ( $t_p = 2/10\mu s$ ) without performance degradation and a minimum  $\pm 30kV$  ESD per IEC61000-4-2 international standard. The low loading capacitance makes the SP4042 ideal for protecting Ethernet interfaces.

### Features

- ESD, IEC61000-4-2,  $\pm 30kV$  contact,  $\pm 30kV$  air
- Lightning, IEC61000-4-5 2nd edition, 120A ( $t_p = 2/10\mu s$ )
- EFT, IEC61000-4-4, 40A ( $t_p = 5/50ns$ )
- Low capacitance of 11pF (TYP) per line
- Low leakage current of 0.1 $\mu A$  (MAX) at 3.3V
- Lead-free and RoHS compliant

### Applications

- 10/100/1000 Ethernet Interfaces
- Customer Premise Equipment (CPE)
- Carrier Class Equipment
- PBX Systems

Life Support Note:

**Not Intended for Use in Life Support or Life Saving Applications**

The products shown herein are not designed for use in life sustaining or life saving applications unless otherwise expressly indicated.

### Absolute Maximum Ratings

Symbol	Parameter	Value	Units
$I_{PP}$	Peak Current ( $t_p=8/20\mu s$ )	95	A
$I_{PP}$	Peak Current ( $t_p=2/10\mu s$ )	120	A
$P_{PK}$	Peak Pulse Power ( $t_p=2/10\mu s$ )	2500	W
$T_{OP}$	Operating Temperature	-40 to 85	°C
$T_{STOR}$	Storage Temperature	-55 to 150	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### Thermal Information

Parameter	Rating	Units
Storage Temperature Range	-55 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 20-40s)	260	°C

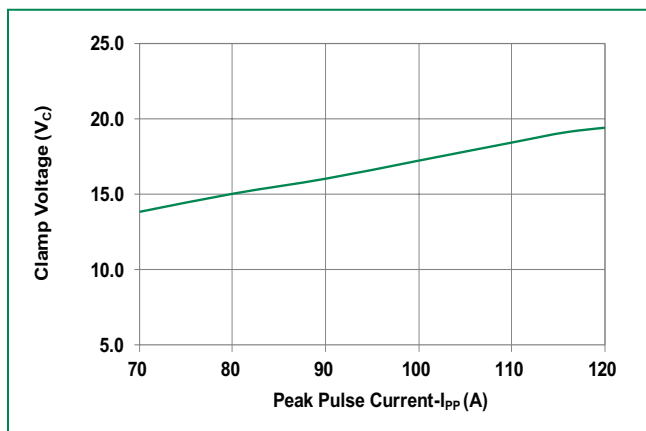
### Electrical Characteristics ( $T_{OP}=25^\circ C$ )

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reverse Standoff Voltage	$V_{RWM}$	$I_R \leq 1\mu A$ , Line to Line			3.3	V
Reverse Breakdown Voltage	$V_{BR}$	$I_T = 1mA$ , Line to Line	3.5			V
Snap Back Voltage	$V_{SB}$	$I_{SB} = 50mA$	2.8			V
Reverse Leakage Current	$I_{LEAK}$	$V_R = 3.3V$ , Line to Line			0.1	$\mu A$
Clamp Voltage, Line to GND <sup>1</sup>	$V_C$	$I_{PP} = 100A$ , $t_p = 2/10\mu s$		17	22	V
Clamp Voltage, Line to Line <sup>1</sup>		$I_{PP} = 100A$ , $t_p = 2/10\mu s$		22	25	V
ESD Withstand Voltage <sup>1</sup>	$V_{ESD}$	IEC61000-4-2 (Contact)	$\pm 30$			kV
		IEC61000-4-2 (Air)	$\pm 30$			kV
Dynamic Resistance, Line to GND <sup>2</sup>	$R_{DYN}$	TLP, $t_p = 100ns$		0.05		$\Omega$
Dynamic Resistance, Line to Line <sup>2</sup>				0.15		$\Omega$
Diode Capacitance <sup>1</sup>	$C_{I/O-GND}$	Line to GND, $V_R = 0V$ , $f = 1MHz$		11	25	pF
	$C_{I/O-I/O}$	Line to Line, $V_R = 0V$ , $f = 1MHz$		5.5	12	pF

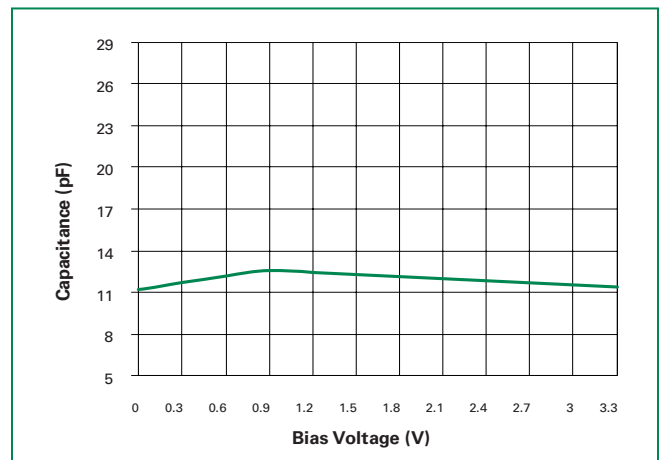
Note: 1 Parameter is guaranteed by design and/or device characterization.

2 Transmission Line Pulse (TLP) test setting : Std.TDRI(50Q),  $t_p=100ns$ ,  $tr=0.2ns$  ITLP and VTLP averaging window: star  $t1=70ns$  to end  $t2=80ns$

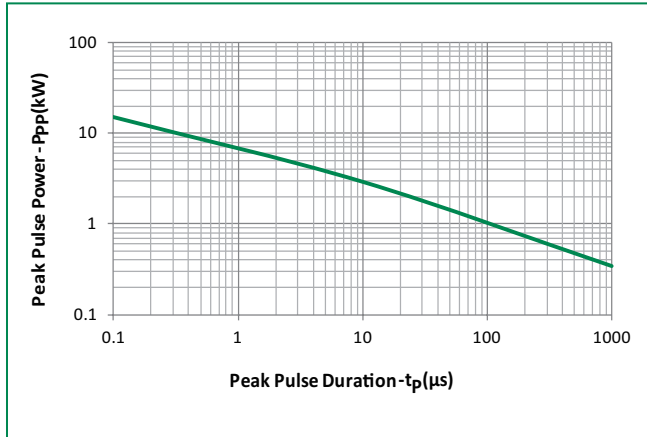
### Wave Form 2/10 $\mu s$ Clamping Voltage vs. Peak Pulse Current (Line to GND)



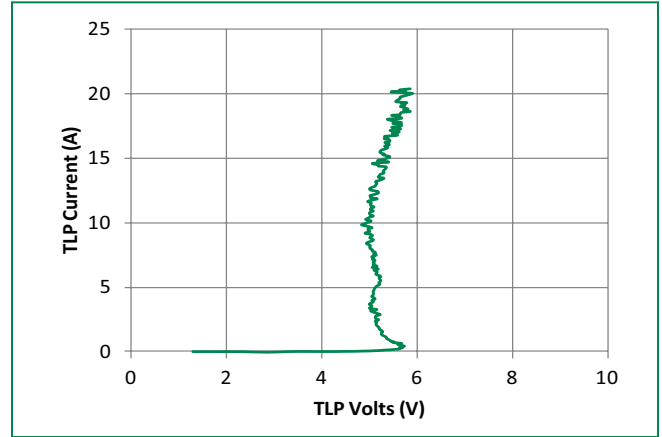
### Capacitance vs. Reverse Bias (Line to GND)



**Non-Repetitive Peak Pulse Power vs. Pulse Time**

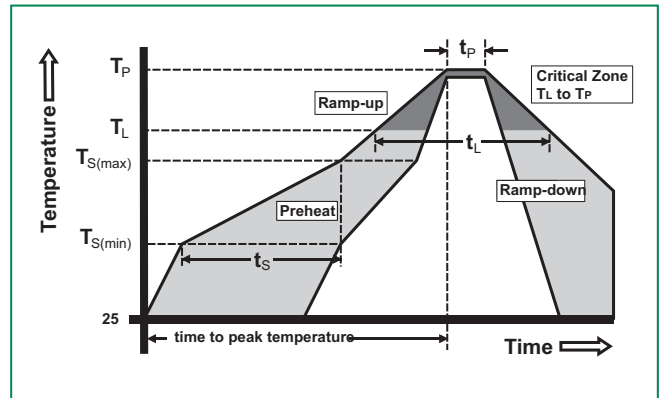


**Positive Transmission Line Pulsing (TLP) Plot (Line to GND)**



**Soldering Parameters**

Reflow Condition	Pb – Free assembly	
Pre Heat	- Temperature Min ( $T_{s(min)}$ )	150°C
	- Temperature Max ( $T_{s(max)}$ )	200°C
	- Time (min to max) ( $t_s$ )	60 – 180 secs
Average ramp up rate (Liquidus) Temp ( $T_L$ ) to peak	3°C/second max	
$T_{s(max)}$ to $T_L$ - Ramp-up Rate	3°C/second max	
Reflow	- Temperature ( $T_L$ ) (Liquidus)	217°C
	- Temperature ( $t_L$ )	60 – 150 seconds
Peak Temperature ( $T_p$ )	260 <sup>+0/-5</sup> °C	
Time within 5°C of actual peak Temperature ( $t_p$ )	20 – 40 seconds	
Ramp-down Rate	6°C/second max	
Time 25°C to peak Temperature ( $T_p$ )	8 minutes Max.	
Do not exceed	260°C	



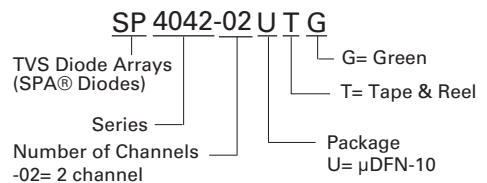
**Product Characteristics**

<b>Lead Plating</b>	Pre-Plated Frame
<b>Lead Material</b>	Copper Alloy
<b>Lead Coplanarity</b>	0.004 inches(0.102mm)
<b>Substrate material</b>	Silicon
<b>Body Material</b>	Molded Epoxy
<b>Flammability</b>	UL 94 V-0

Notes :

1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
5. Package surface matte finish VDI 11-13.

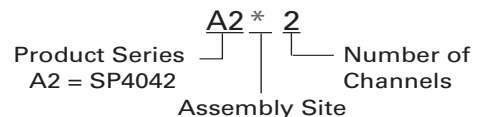
**Part Numbering System**



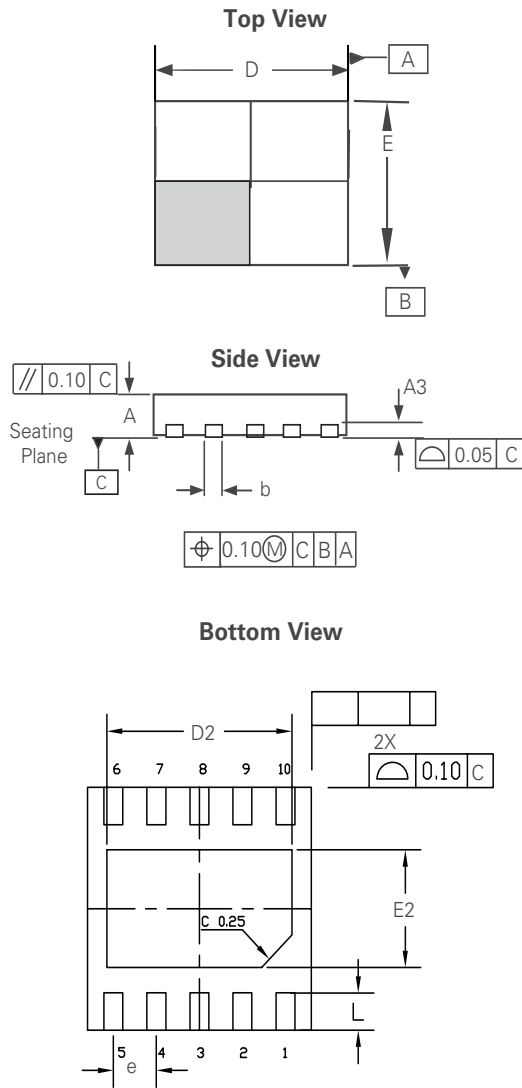
**Ordering Information**

Part Number	Package	Marking	Min. Order Qty.
SP4042-02UTG	$\mu$ DFN-10	A2*2	3000

**Part Marking System**

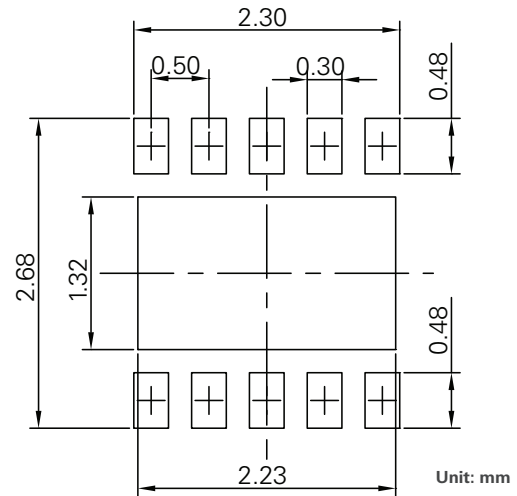


**Package Dimensions —  $\mu$ DFN-10**

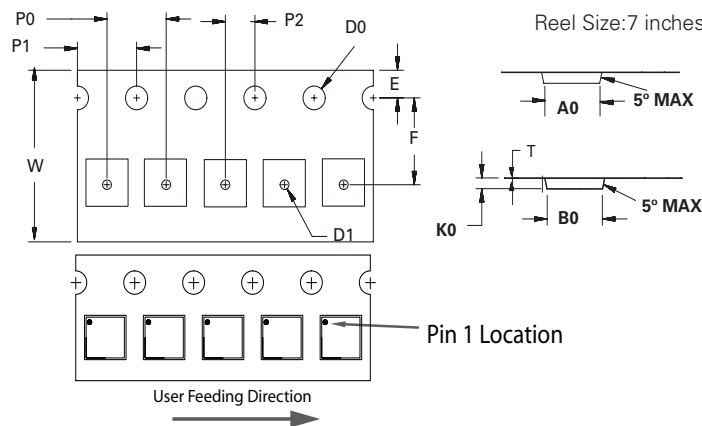


Package	$\mu$ DFN-10 (2.6x2.6mm)					
JEDEC	MO-229					
Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
<b>A</b>	0.45	0.52	0.55	0.018	0.020	0.022
<b>A3</b>	0.127Ref			0.005 Ref		
<b>b</b>	0.17	0.22	0.27	0.006	0.009	0.011
<b>D</b>	2.50	2.60	2.70	0.098	0.102	0.106
<b>D2</b>	2.10	2.15	2.20	0.083	0.085	0.087
<b>E</b>	2.50	2.60	2.70	0.098	0.102	0.106
<b>E2</b>	1.21	1.26	1.31	0.048	0.050	0.052
<b>e</b>	0.50 BSC			0.020 BSC		
<b>L</b>	0.35	0.40	0.45	0.014	0.016	0.018

**RECOMMENDED SOLDER PAD**



**Embossed Carrier Tape & Reel Specification —  $\mu$ DFN-10 (2.6x2.6mm)**



Symbol	Millimeters
<b>A0</b>	2.82 +/- 0.05
<b>B0</b>	2.82 +/- 0.05
<b>D0</b>	Ø1.50 + 0.10
<b>D1</b>	Ø 0.50 + 0.05
<b>E</b>	1.75 +/- 0.10
<b>F</b>	3.50 +/- 0.05
<b>K0</b>	0.76 +/- 0.05
<b>P0</b>	4.00 +/- 0.10
<b>P1</b>	4.00 +/- 0.10
<b>P2</b>	2.00 +/- 0.05
<b>T</b>	0.25 +/- 0.02
<b>W</b>	8.00 + 0.30 /- 0.10