

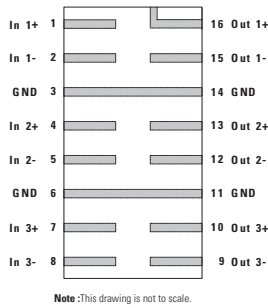
SP5002 6 Channel Common Mode Filter



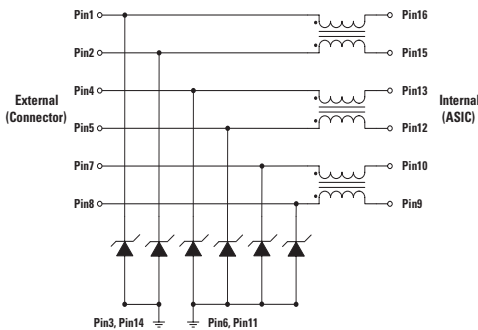
**OBSOLETE** DATE: 12/31/2020 PCN/ECN# ESU270-49  
REPLACED BY: SP5001-04TTG for functional



**Pinout**



**Functional Block Diagram**



**Description**

The SP5002 Series is a highly integrated Common Mode Filter (CMF) providing both ESD protection and EMI common mode noise filtering for systems using high speed differential serial interfaces, such as MIPI D-PHY.

The SP5002 Series can protect and filter three differential line pairs in a small RoHS-compliant TDFN-16 package, with cost and space savings over discrete solutions.

**Features**

- Large differential bandwidth > 2GHz
- High Common Mode Stop Band Attenuation:
  - > 25 dB at 700 MHz
  - > 30 dB at 800 MHz
- ±15kV ESD protection per channel (IEC 61000-4-2 Level 4, contact discharge and ±30kV air discharge)
- TDFN-16 4.00mm × 2.00mm × 0.75mm package with 0.50mm lead pitch
- RoHS-Compliant, Lead-Free packaging
- Moisture Sensitivity Level (MSL-1)

**Applications**

- MIPI D-PHY (CSI-2, DSI, etc) in Mobile Phones and Digital Still Cameras
- HDMI/DVI Display in Mobile Phones

**Absolute Maximum Ratings**

Symbol	Parameter	Value	Units
$I_{DC}$	DC Current Per Line	100	mA
$P_{DC}$	DC Package Power Rating	0.5	W
$T_{OP}$	Operating Temperature	-40 to 125	°C
$T_{STOR}$	Storage Temperature	-55 to 150	°C

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the component. This is a stress only rating and operation of the component at these or any other conditions above those indicated in the operational sections of this specification is not implied.

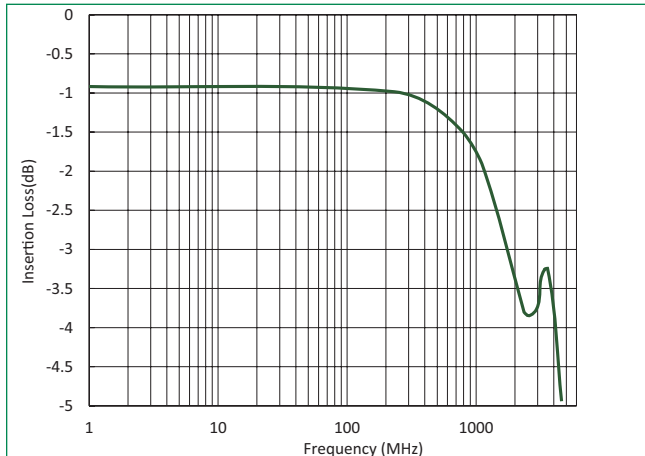
**Electrical Characteristics ( $T_{OP}=25^{\circ}C$ )**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Channel Resistance	$R_{CH}$	Pins 1-16, 2-15, 4-13, 5-12, 7-10, and 8-9		8.0		$\Omega$
Total Channel Capacitance	$C_{TOTAL}$	$V_{I/O} = 1.65V_{DC}$ Reverse Bias; $f=1MHz, 30mV_{AC}$		0.8	1.3	pF
Reverse Standoff Voltage	$V_{RWM}$				5.0	V
Breakdown Voltage	$V_{BR}$	$I_T=1mA$	6.0	8.0	10.0	V
Forward Voltage at $I_F$	$V_F$	$I_F=1mA$	0.4	0.7	1.5	V
Reverse Leakage Current	$I_{LEAK}$	$V_{I/O}=3.3V$		0.01	0.10	$\mu A$
Dynamic Resistance <sup>2,3</sup>	$R_{DYN}$	Positive ( $tp=8/20\mu s$ )		1.3		$\Omega$
		Negative ( $tp=8/20\mu s$ )		0.7		
		TLP, $tp=100ns$ , I/O to GND		0.36		
ESD Withstand Voltage <sup>1,2</sup>	$V_{ESD}$	IEC 61000-4-2 (Contact Discharge)	$\pm 15$			kV
		IEC 61000-4-2 (Air Discharge)	$\pm 30$			kV
Differential Mode Cutoff Frequency <sup>2</sup>	$F_{3dB}$	$Z_{SOURCE}=50\Omega, Z_{LOAD}=50\Omega$		2.0		GHz
Common Mode Stop Band Attenuation <sup>2</sup>	$F_{\sigma}$	$f=800MHz$		30		dB

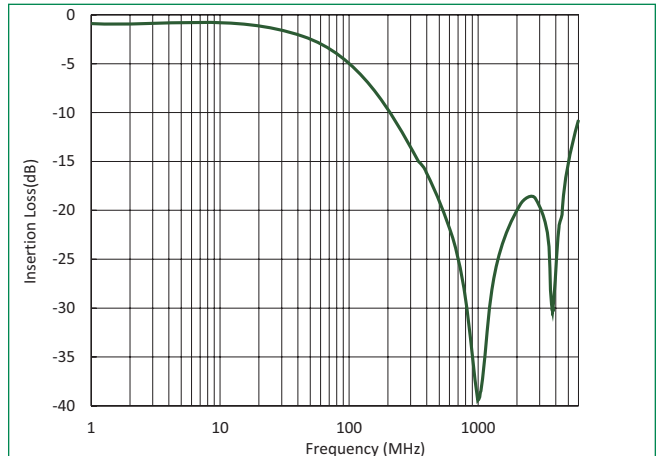
**Notes:**

- ESD zapping at I/O pins (1,2,4,5,7,8) with respect to GND.
- Guaranteed by design.
- Transmission Line Pulse (TLP) with 100ns width and 200ps rise time.

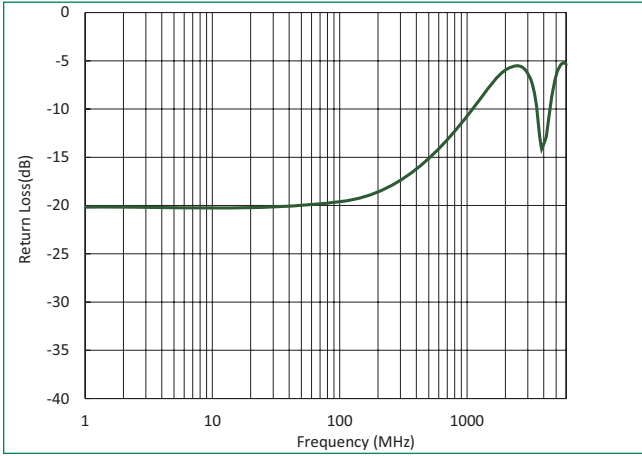
**Differential Mode Attenuation SDD21 vs. Frequency ( $Z_{diff} = 100\Omega$ )**



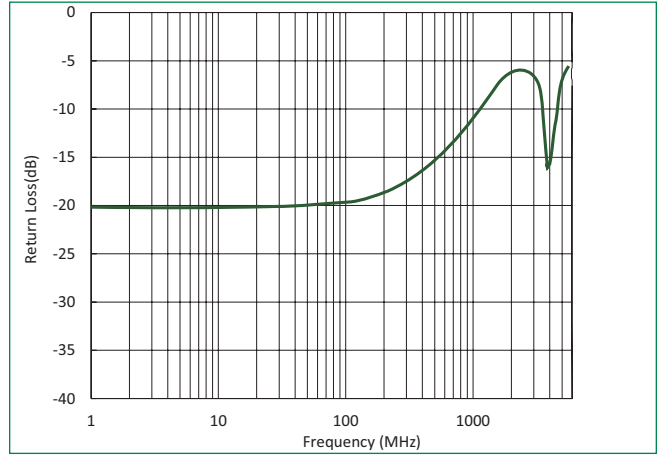
**Common Mode Attenuation SCC21 vs. Frequency ( $Z_{comm}= 50\Omega$ )**



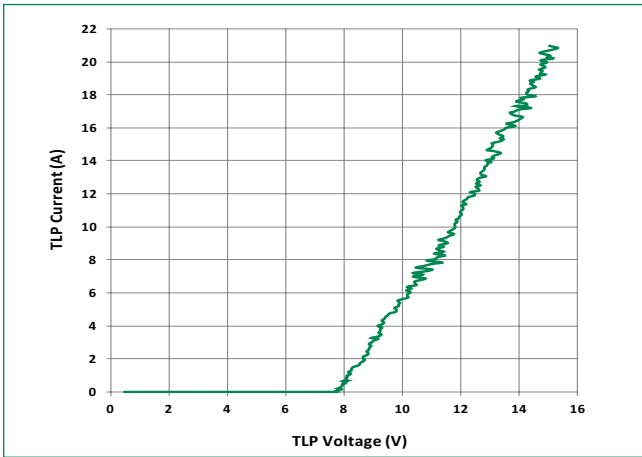
**Differential Return Loss SDD11 vs. Frequency (Zdiff = 100Ω)**



**Differential Return Loss SDD22 vs. Frequency (Zdiff = 100Ω)**

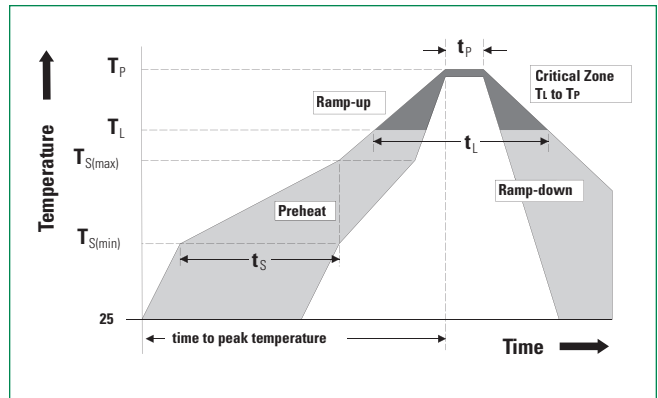


**Transmission Line Pulsing (TLP) Plot**



**Soldering Parameters**

<b>Reflow Condition</b>		Pb – Free assembly
<b>Pre Heat</b>	- Temperature Min ( $T_{s(min)}$ )	150°C
	- Temperature Max ( $T_{s(max)}$ )	200°C
	- Time (min to max) ( $t_s$ )	60 – 180 secs
<b>Average ramp up rate (Liquidus) Temp (<math>T_L</math>) to peak</b>		3°C/second max
<b><math>T_{s(max)}</math> to <math>T_L</math> - Ramp-up Rate</b>		3°C/second max
<b>Reflow</b>	- Temperature ( $T_L$ ) (Liquidus)	217°C
	- Temperature ( $t_L$ )	60 – 150 seconds
<b>Peak Temperature (<math>T_p</math>)</b>		260 <sup>+0.5</sup> °C
<b>Time within 5°C of actual peak Temperature (<math>t_p</math>)</b>		20 – 40 seconds
<b>Ramp-down Rate</b>		6°C/second max
<b>Time 25°C to peak Temperature (<math>T_p</math>)</b>		8 minutes Max.
<b>Do not exceed</b>		260°C



**Product Characteristics**

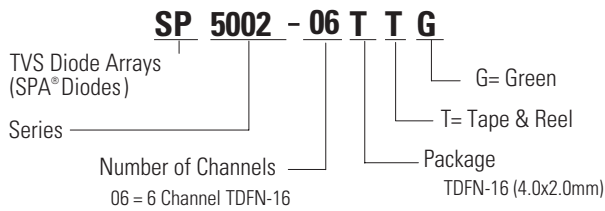
<b>Lead Plating</b>	Pre-Plated Frame
<b>Lead Material</b>	Copper Alloy
<b>Substrate material</b>	Silicon
<b>Body Material</b>	V-0 per UL 94 Molded Epoxy

- Notes:**
1. All dimensions are in millimeters
  2. Dimensions include solder plating.
  3. Dimensions are exclusive of mold flash & metal burr.
  4. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
  5. Package surface matte finish VDI 11-13.

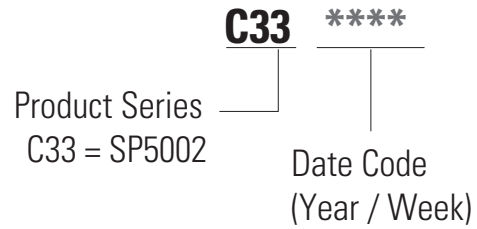
**Ordering Information**

Part Number	Package	Size	Min. Order Qty.
SP5002-06TTG	TDFN-16	4.0x2.0mm	3000

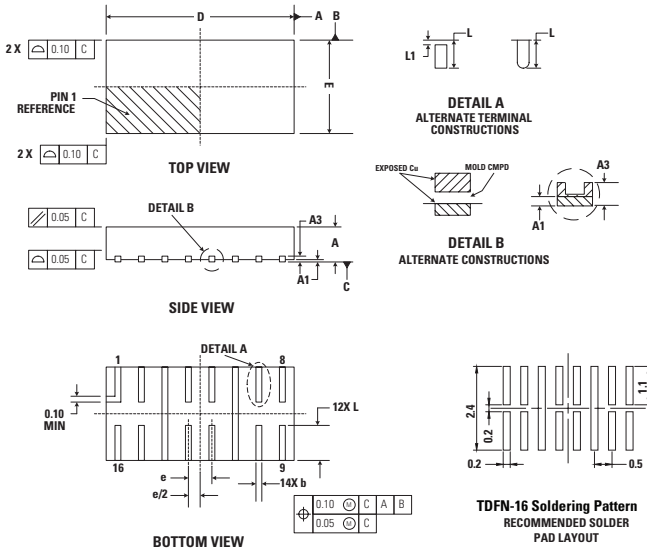
**Part Numbering System**



**Part Marking System**

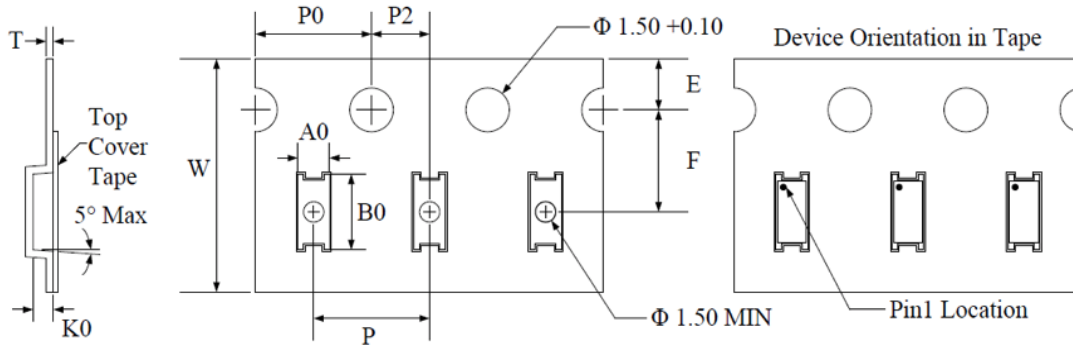


**Package Dimensions – TDFN-16**



Symbol	TDFN-16 JEDEC MO-229			
	Millimeters		Inches	
	Min	Max	Min	Max
<b>A</b>	0.70	0.80	0.028	0.031
<b>A1</b>	0.00	0.05	0.00	0.002
<b>A3</b>	0.20 REF		0.008 REF	
<b>b</b>	0.15	0.25	0.006	0.010
<b>D</b>	3.95	4.05	0.156	0.159
<b>E</b>	1.95	2.05	0.077	0.081
<b>e</b>	0.50 BSC		0.020 BSC	
<b>L</b>	0.70	0.90	0.028	0.035
<b>L1</b>	0.05	0.15	0.002	0.006

**Tape and Reel Specifications**



Symbol	W	A0	B0	K0	E	F	P	P0	P2	T
Dimensions (mm)	12.00 $\pm 0.30$	2.30 $\pm 0.10$	4.27 $\pm 0.08$	1.00 $\pm 0.10$	1.75 $\pm 0.10$	5.50 $\pm 0.05$	4.00 $\pm 0.10$	4.00 $\pm 0.10$	2.00 $\pm 0.05$	0.30 $\pm 0.05$

