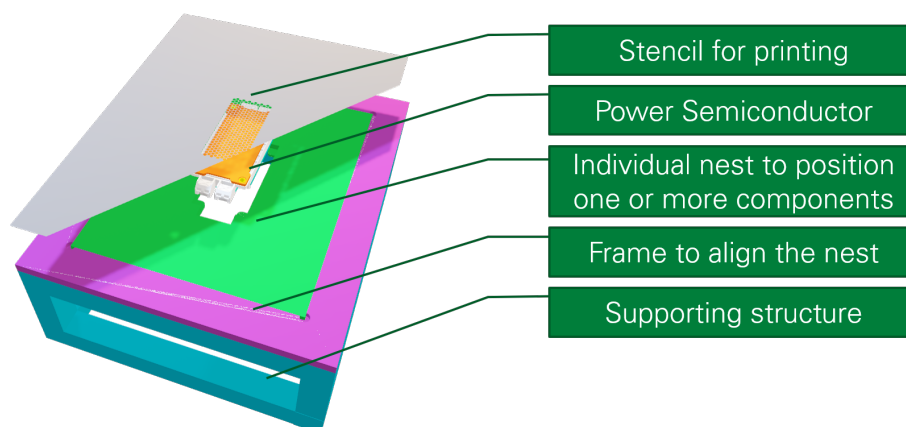


## Basics of Stencil Generation to Apply Thermal Grease to Power Semiconductors

### Objectives

This document outlines how to properly apply Thermal Interface Material (TIM) to power semiconductors using stencils in screen-printing processes. **Figure 1** shows a basic setup to do so.



**Figure 1. Basic Setup to Use Screen-printing for Thermal Interface Material**

### Applications

Any system that features components that need to dissipate heat to properly operate, particularly power electronic designs with large-scale power semiconductors

### Target Audience

This document is intended for all personnel involved in designing and assembling power electronics.

### Contact Information

For more information on the topic, contact the Littelfuse Power Semiconductor team of product and applications experts at [PowerSemiSupport@Littelfuse.com](mailto:PowerSemiSupport@Littelfuse.com)

## Table of Contents

1. Introduction .....	3
2. Generic Stencil Design .....	3
2.1. Stencil for Modules with Exposed DCB-backsides.....	5
2.2. Stencil for Modules with Metal Base Plates.....	5
2.3. Applying Thermal Grease using Screen Printing.....	7
3. Verification and Optimization .....	9
4. Summary .....	9

## List of Figures

Figure 1. Basic Setup to Use Screen-printing for Thermal Interface Material.....	1
Figure 2. Screenshot to Visualize the Reference Settings.....	3
Figure 3. Parameters for Calculating the Fill Factor in a Pattern of Hexagonal Dots.....	4
Figure 4. Sequence of Constructing a Generic Stencil .....	5
Figure 5. Example of an E3-type Power Module and its Thermally Active Area.....	5
Figure 6. Pattern Creation Superimposing the Thermally Active Area and a Regular Pattern.....	6
Figure 7. Power Semiconductor and the Final Stencil Pattern.....	6
Figure 8. Toolset for Manually Printing TIM to Power Modules .....	7
Figure 9. Power Component Positioned in the Nest for Printing.....	7
Figure 10. Adding Centering Pins to Ease Stencil Alignment .....	8

## List of Tables

Table 1: Pattern Parameters .....	3
-----------------------------------	---

## 1. Introduction

The most common root cause of field-failures in power electronic systems is excessive temperature rise. In most cases, the thermal transfer from the power component to the correlating heat sink was disturbed over time. Analysis revealed that either the Thermal Interface Material (TIM) in place degraded or that the material was applied in an unfavorable way.

A lack of thermal interface material as well as applying too much of it can result in too high a thermal resistance. An excess amount can also lead to high stress and damage during mounting, particularly when the power semiconductor features a Direct Copper Bonded (DCB) ceramic as a contact surface.

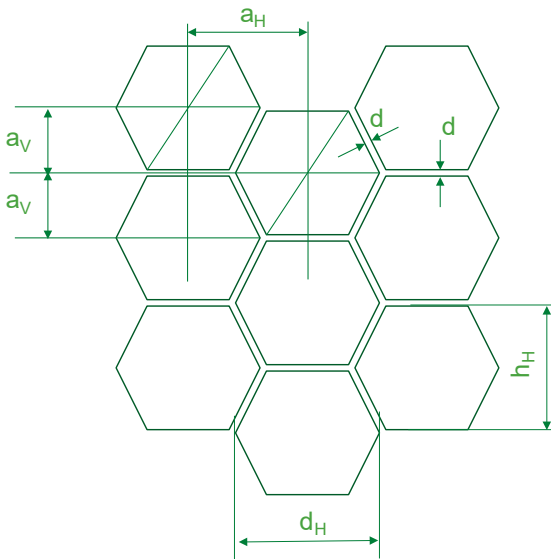
Therefore, when applying thermal grease, one must consider the overall amount, the position, and the thickness of the layer. While the process used to apply the material needs to achieve reproducible results, care must be taken to not contaminate other areas with the TIM. This is particularly important for screws, threads, and areas that later get coated or painted.

Additionally, product specific mounting procedures as given in dedicated application notes must be obeyed to prevent damage due to inadequate handling during mounting and assembly.

## 2. Generic Stencil Design

The stencil is the template that contains the pattern to be printed to the power semiconductor. Thermal grease, unlike solder paste, is not printed as a homogeneous layer. Instead, a pattern of thermal grease is first applied to the power component’s heat transfer surface. That pattern is then uniformly distributed between the thermally active area and the heat sink during the mounting process.

A multitude of patterns can be considered, including regular or non-regular arrangements of circles, squares, or hexagonal dots. In a regular pattern, the distances between the single dots’ centers doesn’t change, as displayed in **Figure 2**. **Table 1** lists the parameters necessary to construct a pattern from hexagonal dots.



**Table 1: Pattern Parameters**

Parameters	Description	Value
$d_H$	Honeycomb diameter	2-5 mm
$d$	Minimum gap between honeycombs	0.25-0.35 mm
$h_H$	Honeycomb height	$h_H = d_H \cdot \frac{\sqrt{3}}{2}$
$a_H$	Horizontal distance center-center	$a_H = \frac{3}{4}d_H + \frac{d\sqrt{3}}{2}$
$a_v$	Vertical distance center-center	$a_v = \frac{1}{2}(h_H + d)$

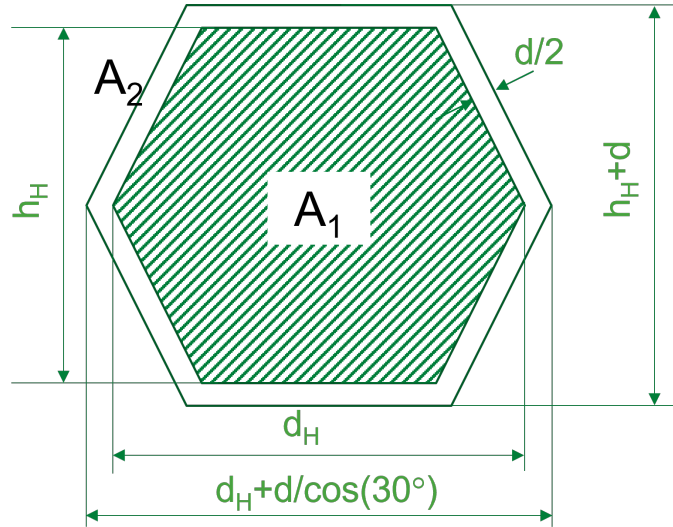
**Figure 2. Screenshot to Visualize the Reference Settings**

A basic stencil design with a homogenous pattern presents a good first approach. Optimization of an initial pattern can be done later to maximize the thermal transfer and minimize the amount of material at the same time. However, such an optimization must consider the power component, the thermal interface material, and the process of application. Depending on the semiconductor in use, chip temperatures can potentially be reduced by 2 to 3 Kelvin with an optimized stencil and TIM pairing.

For the present document, the design guideline to build a generic stencil is described. Such a stencil will work sufficiently with most of the common greases available in the market.

An important parameter to consider is the stencil thickness,  $d_s$ . Though a thin stencil of  $d_s=80$  to  $100\ \mu\text{m}$  may seem favorable, it might not achieve a suitable service life in permanent operation resulting in costly replacements.

Knowing the targeted layer thickness,  $d_{\text{target}}$ , that needs to be achieved, the thickness of the stencil can be derived from the relation of used and total area, the fill factor  $\eta_{\text{fill}}$ . For a homogeneous pattern built from hexagons, the correlation can be seen in **Figure 3**.



**Figure 3. Parameters for Calculating the Fill Factor in a Pattern of Hexagonal Dots**

Knowing the dots' dimensions and the gap between the dots, **Equation 1** and **Equation 2** can be used to calculate the fill factor and the stencil thickness.

Fill Factor 
$$\eta_{\text{fill}} = \frac{A_1}{A_2} = \frac{d_H^2}{\left(d_H + \frac{2 \cdot d}{\sqrt{3}}\right)^2} \quad 1$$

Stencil Thickness 
$$d_s = \frac{d_{\text{target}}}{\eta_{\text{fill}}} = d_{\text{target}} \cdot \frac{A_2}{A_1} \quad 2$$

In case the stencil thickness returns too low a value, decreasing the dots' diameter and/or increasing the distance between dots changes the thickness of the stencil towards higher values. Generally, a stencil thickness of  $100$  to  $125\ \mu\text{m}$  has proven to achieve both good thermal results as well as sufficiently long service life. Depending on the grease in use and the power semiconductor component, an even higher thickness might be considered. As a rule of thumb, stencil thicknesses that reach or exceed  $200\ \mu\text{m}$  should be avoided.

The final stencil is manufactured from stainless steel using laser- or water-jet-cutting techniques. It is important to ensure a clean cut without burrs, as these would lead to quick wear of squeegees, scratch-marks on the power component, and/or particles in the thermal interface material after printing.

## 2.1. Stencil for Modules with Exposed DCB-backsides

The simple procedure given in **Figure 4** can be followed to construct a stencil. Once the dot-size and distance are defined, a regular pattern is generated which is larger in size than the DCB of the power component. The DCB-size can be taken from the component's datasheet and then intersected with the pattern. Adding a surrounding boundary to the result finalizes the stencil.

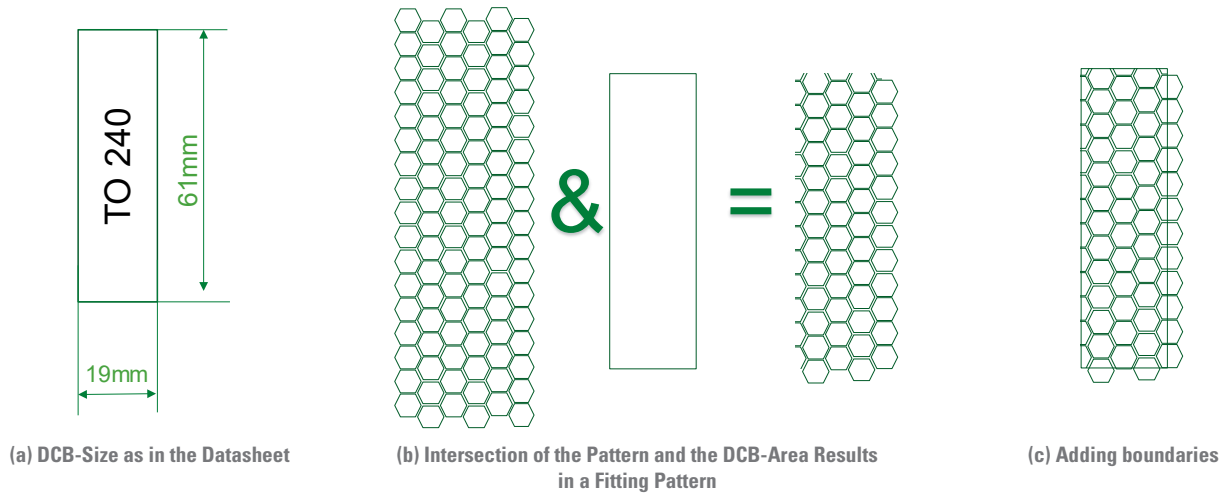


Figure 4. Sequence of Constructing a Generic Stencil

## 2.2. Stencil for Modules with Metal Base Plates

In case a module features a metal base plate, care needs to be taken to keep the area around the screws free of thermal grease. Due to the high forces applied by screws, these areas feature a direct metal-to-metal contact which has a high thermal conductivity. Any grease applied here would be detrimental for the setup in thermal aspects. As grease in these areas could also be displaced over time, the reduction of the layer height could lead to a loss of mounting torque. This too is prevented by keeping these zones free of TIM.

**Figure 5** gives an example, highlighting the thermally active area and the keep-out-zones for an E3-type power module.

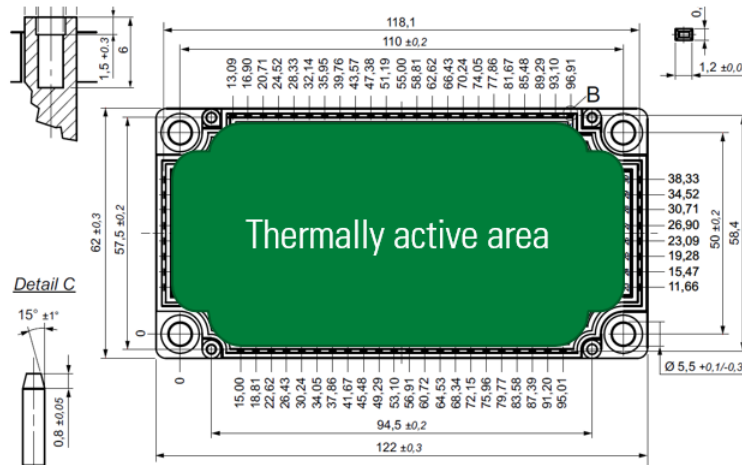
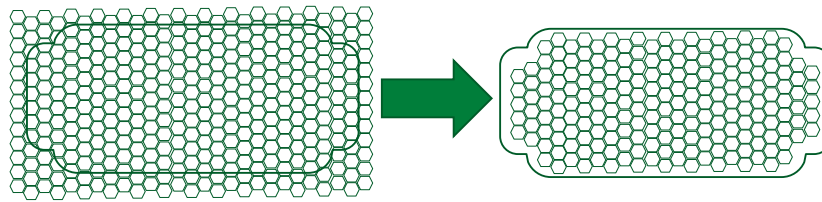


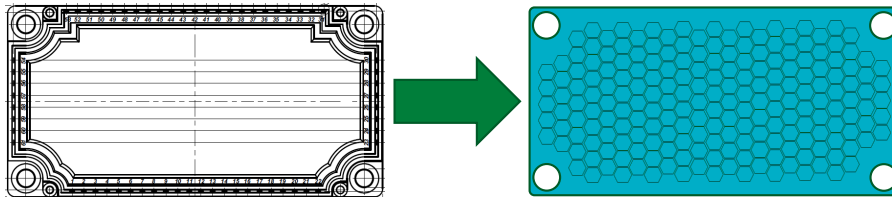
Figure 5. Example of an E3-type Power Module and its Thermally Active Area

Similar to the approach to modules without metal base plates, the boundary of the thermally active area and a pattern of choice are superimposed. This allows removal of the dots that are not necessary, as depicted in **Figure 6**.



**Figure 6. Pattern Creation Superimposing the Thermally Active Area and a Regular Pattern**

Afterwards, a comparison of the power semiconductor and the generated pattern can be done to verify that the area in question is sufficiently covered. For the E3-type module used for the example, this comparison is given in **Figure 7**.



**Figure 7. Power Semiconductor and the Final Stencil Pattern**

In **Figure 7**, it is also visible that the screw position in the corners remains clear of thermal grease as recommended.

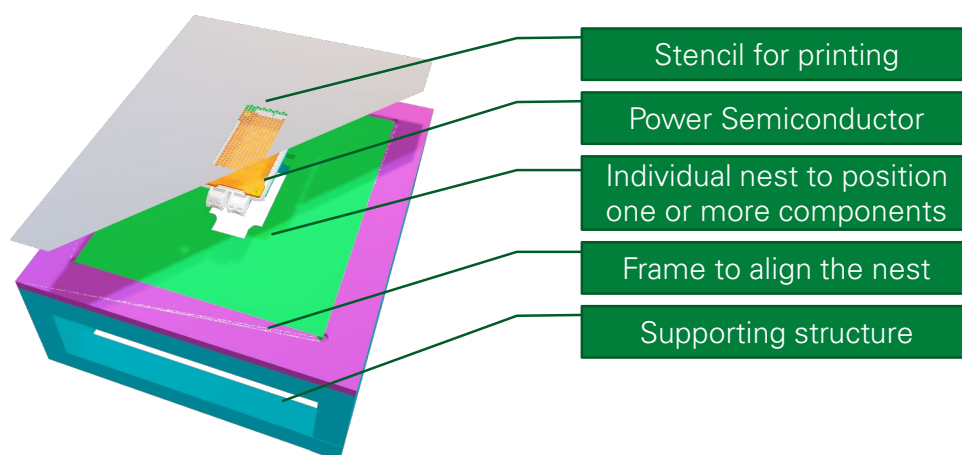
## 2.3. Applying Thermal Grease using Screen Printing

Screen printing turns out to be the most reliable process when applying TIM to power modules. Using brushes, putty-knives, or other mechanical tools does not lead to a reproducible process with the correlating quality requirements.

The process of applying grease to a power device needs to be considered individually, depending on the use-case:

- For repairs in the field, manually applying thermal grease to a single module or a few modules may be desired
- In a lab, a quick way of applying grease to potentially a few dozens of modules for testing may be necessary
- In mass production, a fast, safe, and reliable process is needed, potentially fully automated

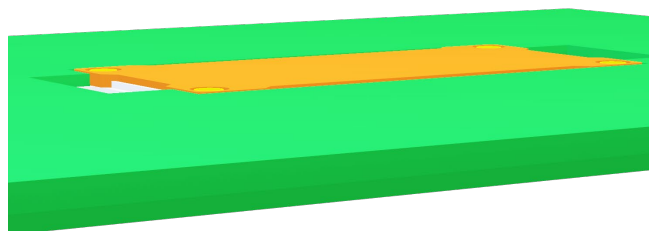
Depending on the number of modules to be handled, manual, semi-automated, or fully automated processes come to mind. For the scope of this document, a manual process is in focus, which can be used in the lab or in low-volume production. Even though manual, such a process is good enough to process several hundred modules per day. The process involves a dedicated screen-printing toolset, as displayed in **Figure 8**.



**Figure 8. Toolset for Manually Printing TIM to Power Modules**

The basic concept is to use the supporting structure with the frame to hold a nest in a fixed position. This way, the position of the power component is well defined and can be aligned with the stencil easily. It is also possible to create a nest for different types of modules, several modules in a single nest, and even combine different modules in one nest to optimize the process accordingly.

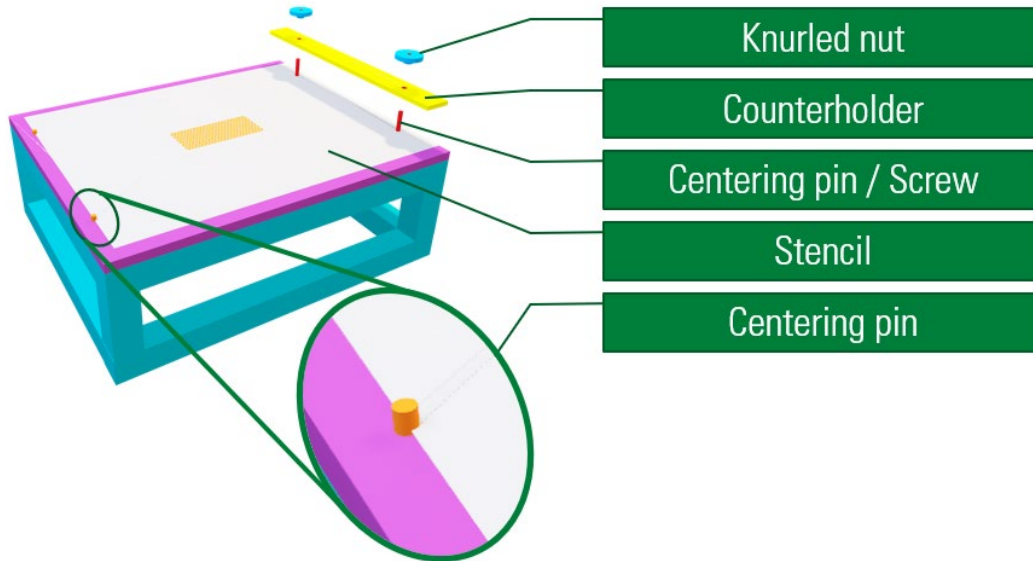
The nest itself is designed to hold the power semiconductor such that the surface to be printed is elevated from the nest's surface slightly, as can be seen in **Figure 9**. An elevation of a fraction of a millimeter is sufficient.



**Figure 9. Power Component Positioned in the Nest for Printing**

Once the stencil is applied, this difference ensures that the stencil is in tight contact with the surface to be printed. This leads to sharp edges and the thermal grease isn't smeared between the stencil and the module. In turn, intervals between cleaning get prolonged and the printed result remains of high quality.

It is advisable to include well-defined and precise reference positions in the frame and the stencil to self-align the stencil and the printing toolset. This reduces the time to set up the toolset when changing the module type or the stencil in use. Typically, precisely ground centering pins are used for this purpose, as pictured in **Figure 10**.



**Figure 10. Adding Centering Pins to Ease Stencil Alignment**

Clamping the stencil on one side only enables lifting it after printing to easily remove the power device from the toolset. For manual working, it is beneficial to include a lever to easily lift the printed device from the nest.



### 3. Verification and Optimization

Typically, a generic stencil works quite well with most thermal interface materials that come as paste-like substances. Still, it is advisable to verify the stencil in mechanical and thermal aspects and potentially improve a first design after evaluation.

Mechanically, the features to check include:

- Does the squeegee fill the dots properly? Depending on the combination of dot-diameter, stencil thickness, TIM viscosity, and temperature, the dots of the stencil may get filled incompletely or material is squeezed out of the dots during printing.
- Stencil thickness should exceed 100µm to achieve a suitable service lifetime
- Is the pattern printed to the proper position?
- Does material get squeezed out from below the module after a few hours of operation? If so, too much material was applied, which may lead to mechanical stress during mounting. It also means that material is wasted, and the thermal transfer is inferior to what is possible. If no material gets squeezed out, thermal verification is needed to ensure that adequate material was applied.

Thermal investigations can include:

- A measurement of the thermal resistance from the chips' junction to the heat sink
- A temperature measurement using an IR-camera to see the thermal development and the chip temperature within the power module. Such a measurement also gives a deep insight into the paths thermal energy takes.
- Long-term tests regarding wear and aging of the thermal interface material in use

Once a generic stencil achieves the desired result, optimization can be done if required. Criteria for optimization can focus on improving the initial thermal performance, the long-term stability, or the reduction of TIM to the minimum needed.

With some thermal interface materials, the material cost can be quite high. Saving even fractions of grams on a larger number of modules helps reduce the cost. Therefore, reducing the amount of material in certain areas can be considered. A reduction can be achieved by stretching the printed pattern or by varying the diameter of individual dots.

Particularly for modules with metal base plates, optimization can involve considering the macroscopic shape of the base plate and local application of TIM in higher density to fill cavities. These cavities can appear in the area of the DCBs' centers due to the thermal processes conducted during manufacturing, including soldering and potting.

### 4. Summary

An accurate stencil is a prerequisite to conduct the precise application of thermal interface material using a screen-printing process. As the process must consider the thermal interface material in use as well as the power semiconductor, it is difficult for component manufacturers to provide a stencil for each component that works as demanded.

With the procedures introduced in this Application Note, creating a stencil that achieves good results with most of the greases available in the market becomes possible. Optimization can be done depending on the individual targets to be achieved.

**Disclaimer Notice:** Information furnished is believed to be accurate and reliable. However, users should independently evaluate the suitability of and test each product selected for their own applications. Littelfuse products are not designed for, and may not be used in, all applications. Read complete Disclaimer Notice at <http://www.littelfuse.com/disclaimer-electronics>.