LEB-0023
IX4352NE Gate Driver Evaluation Board

Introduction

The Littelfuse IX4352NE is 9 A single gate driver optimized for driving Si and SiC-MOSFETs as well as high power IGBTs. To minimize switching losses, the driver allows source and sink peak currents of up to 9 A. With an internal charge pump regulator, the driver provides a user-selectable negative gate drive bias. It enables the design of a driver stage tailored to the specific power semiconductor without putting additional effort into the gate drive power supply. The driver offers short-circuit protection of the power semiconductor through integrated desaturation detection and soft-shutdown function. The purpose of this user manual is to explain the design and use of the Littelfuse IX4352NE gate driver evaluation board as displayed in Figure 1. Equipped with signal and power supply isolation, the board simplifies driver evaluation under different conditions.

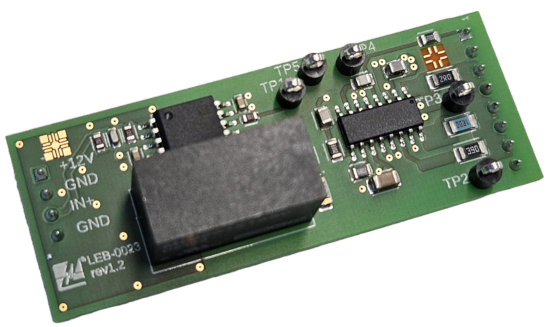

Figure 1. IX4352NE gate driver evaluation board

The evaluation board is part of the Littelfuse gate driver evaluation platform for testing gate drivers with various power semiconductors. Pin headers enable easy integration into existing test setups. Additionally, the platform contains different mainboards, that allow immediate testing and comparison of Littelfuse gate drivers with various power semiconductors. All parts are available from Littelfuse upon request.

Features

Device IX4352NE:

- Separate 9 A peak source/sink outputs
- Internal charge pump regulator for adjustable negative gate drive bias
- Desaturation detection with soft shutdown output
- Under voltage lockout (UVLO)
- Thermal shutdown
- Open drain FAULT output

Evaluation Board:

- Single primary side 12 V power supply
- Isolated DC-DC converter with 15 V output voltage
- On-board gate resistors
- 5000 V_{RMS} – rated digital isolator
- Negative gate drive voltage rail with adjustment option
- Defined creepage of 6 mm between primary and secondary circuit

Target Audience

This user manual is intended for engineers working on power electronics hardware design and investigating optimal driver solutions for their applications.

Contact Information

For more information on the evaluation board and application support, contact the Littelfuse Power Semiconductor team of product and applications experts: PowerSemiSupport@Littelfuse.com

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Important Notes

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1. Overview

The block diagram of the evaluation board is depicted in Figure 2. It contains an isolated DC-DC converter MEJ2S1215SC from Murata Power Solutions (U3) providing isolated 15 V gate driver supply. On primary and secondary side, two 5 V regulators (U4, U5) supply the ADuM210N signal isolator (U3). The output signal of the signal isolator serves as input signal for the IX4352NE driver IC, which delivers sink and source output currents of up to 9 A to the power semiconductor's gate.

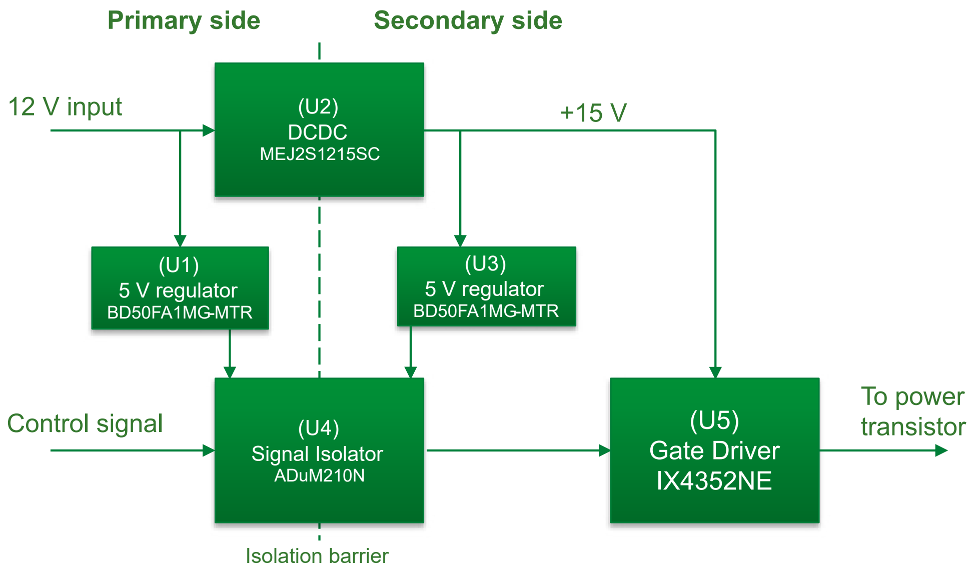

Figure 2. IX4352NE evaluation board block diagram

Table 1 contains the operating conditions of the evaluation board.

Table 1. Operating conditions of the IX4352NE evaluation board

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
V_{CC}	Board supply voltage	11	12	13	V
$V_{Control}$	Control signal input voltage	–	5	5.5	V
V_{IH}	Control signal input voltage high threshold	–	3.5	–	V
V_{IL}	Control signal input voltage low threshold	–	1.5	–	V
I_{OUTSRC}, I_{OUTSNK}	Output peak current	–	–	±9	A
$I_{OUTSOFT}$	Soft turn off peak current	–	–	1	A
dv/dt	Voltage change rate secondary to primary side(1)	–	–	75	V/ns
d_{Creep}	Creepage distance primary to secondary side	–	6	–	mm
d_{Creep}	Clearance distance primary to secondary side	–	6	–	mm
T_{AMB}	Operation ambient temperature	0	25	50	°C

Note:
(1) Based on digital isolator ADuM210N datasheet values

2. Pin Assignments

Table 2 describes the electrical connections of the evaluation board. A 4-terminal pin header is used to connect the PCB on the primary side. On the secondary side, the evaluation board is connected via an 8-terminal pin header. Additionally, five test points are available to record driver signals during operation.

Table 2. Pin assignments of the IX4352NE evaluation board

Connector Name	Pin Number	Pin Name	Description
X1	01	+12 V	Positive 12 V supply primary side
X1	02	GND	Primary side reference
X1	03	IN_+	Driver input signal
X1	04	GND	Primary side reference
X2	01	DESAT_FB	Feedback pin for the driver's desaturation detection. DESAT-Diodes must be placed externally
X2	02	VEE_HV	Gate-loop return path
X2	03	OUT_GATE	Gate output
X2	04	VEE_HV	Gate-loop return path
X2	05	OUT_GATE	Gate output
X2	06	VEE_HV	Gate-loop return path
X2	07	OUT_GATE	Gate output
X2	08	RES	Reserved pin
–	–	TP1	IX3407B positive input test point
–	–	TP2	IX3407B negative input test point
–	–	TP3	Gate connection test point
–	–	TP4	Gate-loop return path test point
–	–	TP5	Gate driver fault output test point

3. Schematics

Figure 3 illustrates the evaluation board's schematic. The upper part of the circuit displays the power supply for the digital isolator ADuM210N and the gate driver IX4352NE. The MEJ2S1215SC DC-DC converter provides isolated driver supply of +15 V. LED1 indicates the presence of the gate driver supply voltage.

The lower part of the schematic depicts the signal isolator and the IX4352NE driver stage. A low-pass filter is connected to the input side of the signal isolator. Depending on the input signal quality, it can be adjusted by the user. The negative driver supply voltage rail is set by the voltage divider of R1 and R2 and is defined by Equation (1).

$$V_{SS} = -4.55\,\text{V} \cdot (R2/R1) + 0.11\,\text{V} \tag{1}$$

In standard configuration, the board is equipped with resistor values of R1 = 33 kΩ and R2 = 68 kΩ, which leads to a negative supply voltage of −9.3 V. If the voltage needs to be adjusted, the voltage divider can be adapted accordingly with the boundary condition R1+ R2 ~ 100 kΩ.

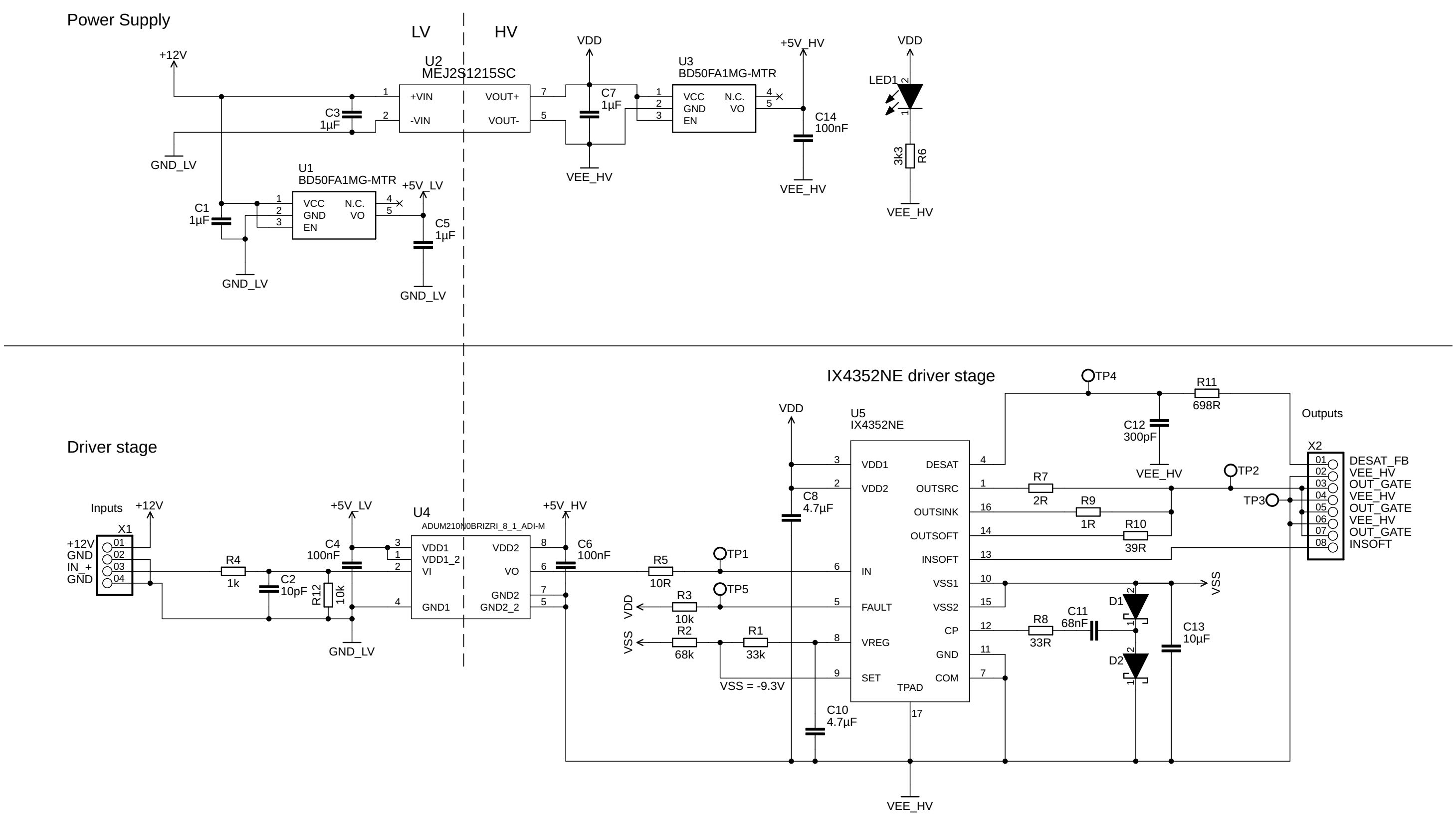

Figure 3. IX4352NE evaluation board schematics

Depending on the power semiconductor in use and the required gate current, the gate resistors for turn-on, turn-off, and soft shutdown can be adjusted. To prevent higher voltages from being looped through the evaluation board, the decoupling diodes of the desaturation detection must also be placed outside the evaluation board. There are external decoupling diodes for the desaturation detection circuit on the available gate driver evaluation mainboards.

4. Bill of Materials

Table 3 lists all the components used on the evaluation board.

Table 3. Bill of materials for the IX4352NE evaluation board

Item	Quantity	Reference	Value	Description	Manufacturer	MPN
1	3	C4, C6, C14	100 nF	Cap 100 nF 25 V 10 % X7R 0603	-generic-	–
2	1	C2	10 pF	Cap 10 pF 25 V 10 % C0G 0603	-generic-	–
3	1	C13	10 µF	Cap 10 µF 50 V 10 % X7R 1206	-generic-	–
4	4	C1, C3, C5, C7	1 µF	Cap 1 µF 50 V 10 % X7R 0805	-generic-	–
5	2	C8, C10	4.7 µF	Cap 4.7 µF 50 V 10 % X7R 0805	-generic-	–
6	1	C11	68 nF	Cap 68 nF 50 V 10 % X7R 0805	-generic-	–
7	1	C12	300 pF	Cap 300 pF 50 V 1 % C0G 0805	-generic-	–
8	1	R5	10 Ω	Res 10 Ω 10 % 0603	-generic-	–
9	2	R3, R12	10 kΩ	Res 10 kΩ 10 % 0603	-generic-	–
10	1	R9	1 Ω	Res 1 Ω 1 % 1206	-generic-	–
11	1	R4	1 kΩ	Res 1 kΩ 10 % 0603	-generic-	–
12	1	R7	2 Ω	Res 2 Ω 1 % 1206	-generic-	–
13	1	R8	33 Ω	Res 33 Ω 10 % 0805	-generic-	–
14	1	R1	33 kΩ	Res 33 kΩ 1 % 0805	-generic-	–
15	1	R10	39 Ω	Res 39 Ω 1 % 1206	-generic-	–
16	1	R6	3.3 kΩ	Res 3.3 kΩ 10 % 0805	-generic-	–
17	1	R2	68 kΩ	Res 68 kΩ 1 % 0805	-generic-	–
18	1	R11	698 Ω	Res 698 Ω 0.1 % 0805	-generic-	–
19	1	LED1	–	LED green 1206	Wuerth Elektronik	156120GS75300
20	1	U4	–	Digital isolator 5 kV	Analog Devices	ADUM210N0BRIZ
21	2	U1, U3	–	LDO Voltage Regulators 5 V/0.1 A	ROHM Semiconductor	BD50FA1MG-MTR
22	1	U5	–	9 A Low side gate driver	Littelfuse	IX4352NE
23	1	U2	–	Isolated DC-DC 12 V/15 V	Murata Power Solutions	MEJ2S1215SC
24	2	D1, D2	–	Schottky Diode 40 V/3 A	Nexperia	PMEG4030ETRX
25	1	X1	–	Pin header 0.1" pitch 4-pin	Samtec	HTSW-104-05-G-S
26	1	X2	–	Pin header 0.1" pitch 8-pin	Samtec	HTSW-108-05-G-S
27	5	TP1, TP2, TP3, TP4, TP5	–	Testpoint THT	Keystone	5006

5. Isolation Ratings

The isolation between the primary and secondary sides of the circuit is provided by the DC-DC converter U2 and the digital isolator U4. The DC-DC converter provides high voltage isolation of up to 5200 VDC with an isolation capacitance of 4 pF. The ADUM210N0 digital isolator provides high voltage isolation of up to 5000 V_{RMS} with an isolation capacitance of 2 pF. For further details on isolation capability of the devices, please view the datasheets of the MEJ2S1215SC and the ADUM210N0.

The creepage and clearance distances on the PCB between the primary and secondary side are 6 mm.

6. PCB Layout

Figures 4 to 7 display the four copper layers of the PCB.

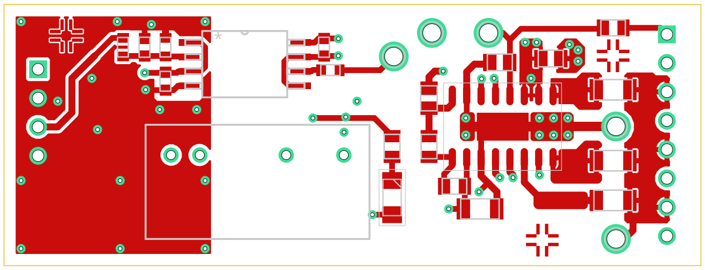

Figure 4. PCB top layer

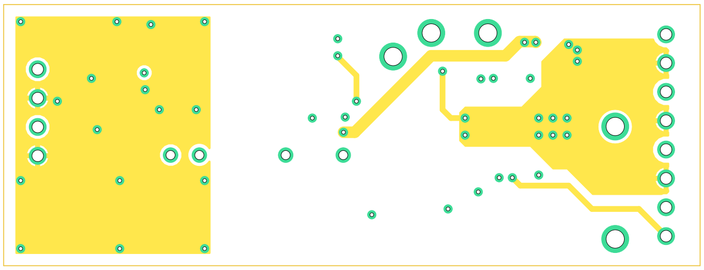

Figure 5. PCB layer 2

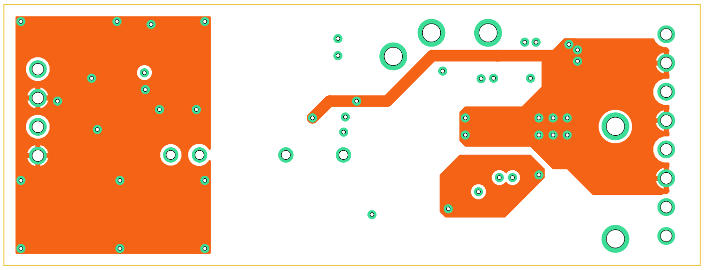

Figure 6. PCB layer 3

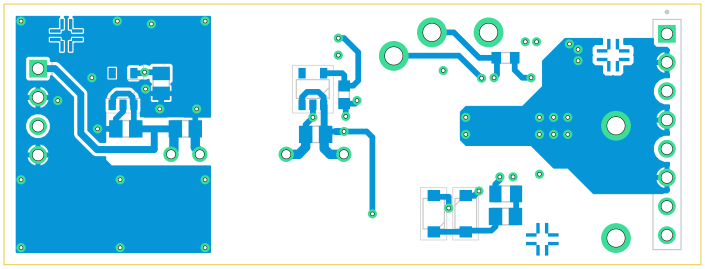

Figure 7. PCB bottom layer

7. PCB Assembly Data

Figure 8 and Figure 9 show the PCB assembly, including the mechanical dimensions of the evaluation board in millimeters.

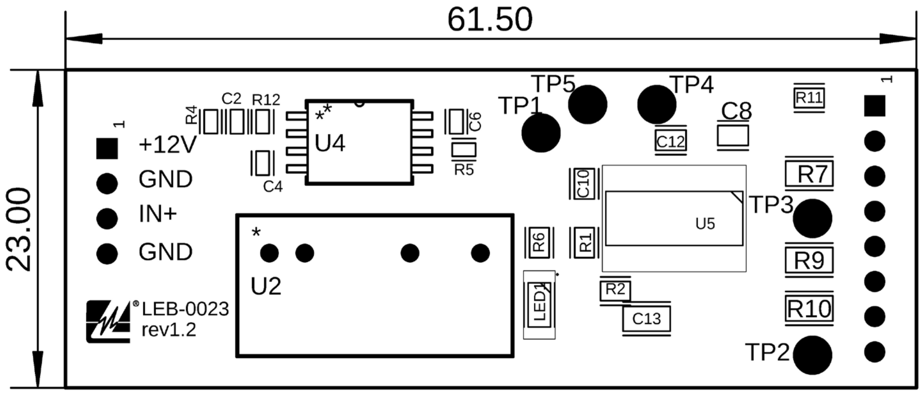

Figure 8. PCB top assembly and dimensions

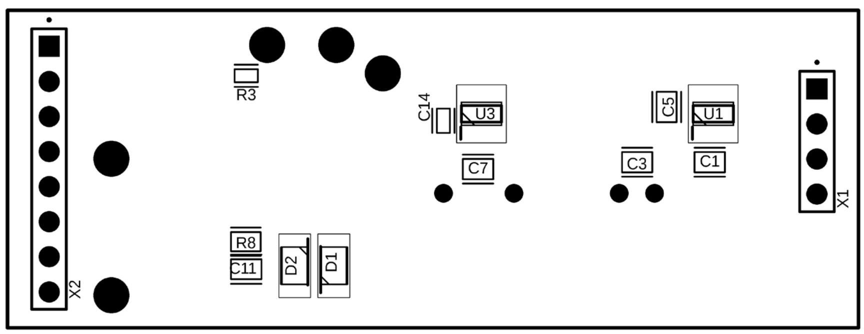

Figure 9. PCB bottom assembly (mirrored view)

8. Measurements

The IX4352NE evaluation board was mounted on the LEB-0025 gate driver evaluation platform mainboard for TO-247-3L packages. The setup was used to conduct double-pulse tests driving Littelfuse IXYH50N65C3H1 IGBTs with a driver supply voltage of +15/-9 V. Figure 10 and Figure 11 depict turn-off and turn-on events of the IGBT.

During the turn-off event of the IGBT, the gate voltage decreases, initiating the turn-off process. Due to a low 2 Ω turn-off gate resistance and characteristics of the IXYH50N65C3H1 IGBT, an extended miller-plateau is absent, and the measured gate voltage directly follows the collector-emitter voltage. Existing stray inductances in the switching cell cause an overvoltage across the IGBT of 100 V. An under swing of the gate-emitter voltage to approximately -18 V occurs during turn-off below the applied gate driver voltage of -9 V. This is caused by two effects. The negative di/dt of the emitter current induces a voltage across the stray inductance in the package's emitter current path. In addition, the negative dv/dt of the collector-emitter voltage after the turn-off voltage peak feeds back to the gate via the miller capacitance leading to a further reduction in the measured gate voltage. This effect can be dampened by using a higher gate resistance value and slowing down the switching speeds. However, since the gate-emitter voltage swing does not exceed the datasheet maximum values, this behavior is not critical.

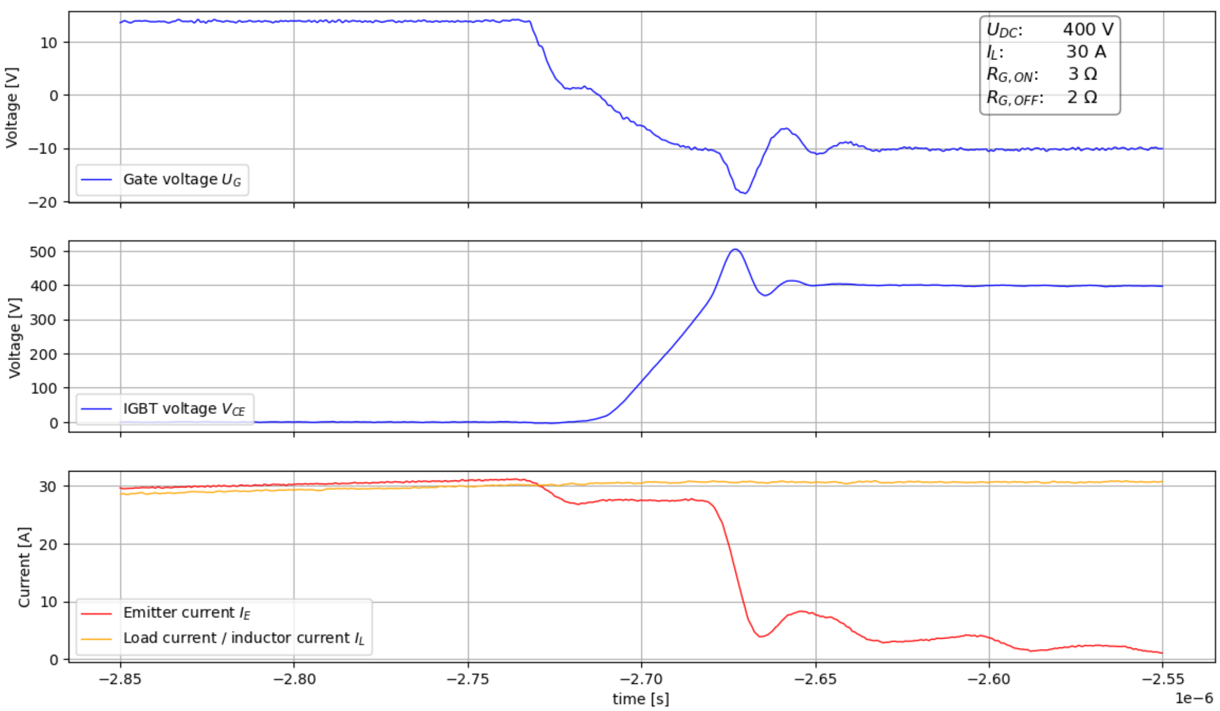

Figure 10. IXYH50N65C3H1 turn-off event at 30 A collector current driven by the IX4352NE

When the IGBT is turned on, an effect like that for turn-off can be observed. Due to the driver's high current capability and low gate resistance, the gate-emitter voltage quickly reaches the positive voltage rail before the collector-emitter voltage drops. The emitter-current begins to rise and an overcurrent of approximately 30 A occurs, which is attributed to the reverse recovery of the free-wheeling diode. The gate voltage temporarily drops due to the negative dv/dt of the collector-emitter voltage and the negative di/dt of the emitter current.

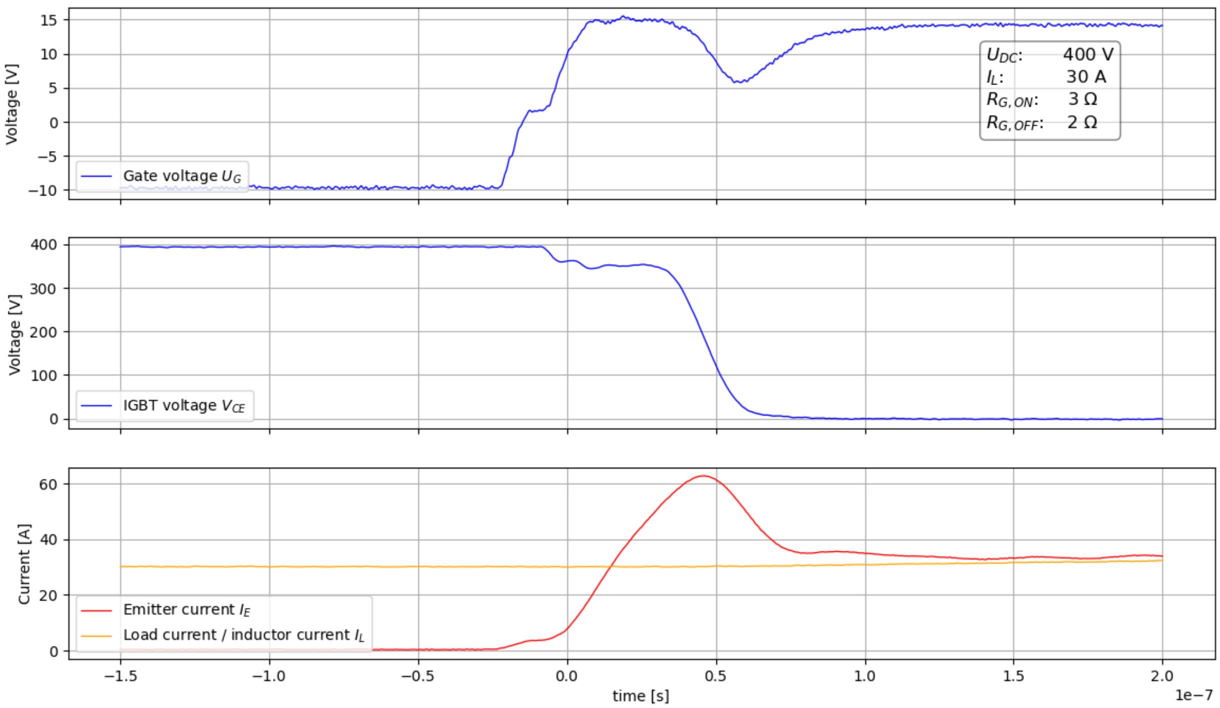

Figure 11. IXYH50N65C3H1 turn-on event at 30 A collector current driven by the IX3407B

To evaluate the desaturation feature of the gate driver, an external 800 µF capacitor was connected to the mainboard to ensure a stable DC-Link voltage. The high-side switch on the mainboard was manually shorted. Figure 12 illustrates the short circuit test result. Upon activation, the IGBT enters desaturation immediately, limiting the collector current to a peak value of approximately 430 A. With a blanking capacitor of 150 pF, the blanking time for desaturation turn-off is set to 2.5 µs. After this period, the gate driver employs its soft turn-off mechanism to safely deactivate the IGBT. The gate driver's fault output indicates the short circuit event by grounding the fault pin.

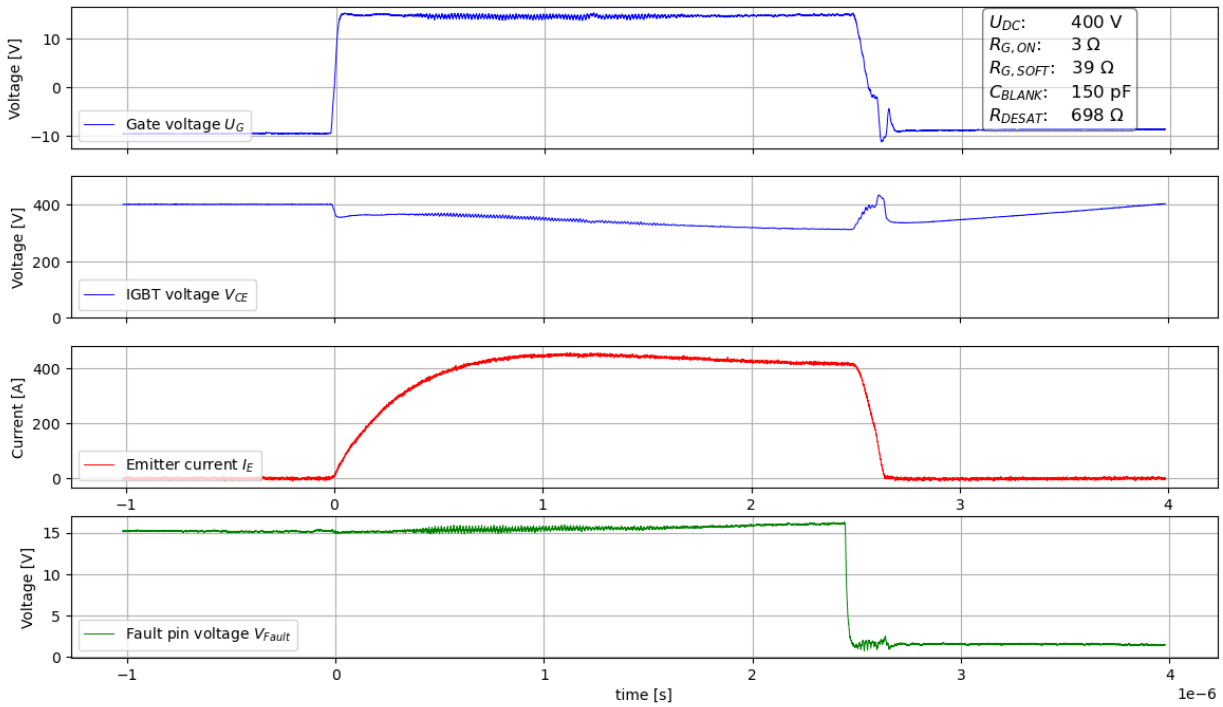

Figure 12. IXYH50N65C3H1 short circuit test with high-side switch manually shorted

Revision History

Date	Revision	Changes
April 2025	1.0	Initial Release