LEB-0027
IXDD609SI Gate Driver Evaluation Board

Introduction

The Littelfuse IXDD609SI is a 9 A single gate driver capable of driving different power semiconductors for minimized switching loss at high switching frequencies. With output currents of up to 9 A, the driver is capable of effectively handling high gate charges. With low propagation delay times and matched rise and fall times, the driver is specially designed for applications where the control timing must be exceptionally precise. The purpose of this application note is to explain the design and use of the Littelfuse IXDD609SI gate driver evaluation board as displayed in Figure 1. Equipped with signal and power isolation, the board allows driver evaluation under laboratory test conditions.

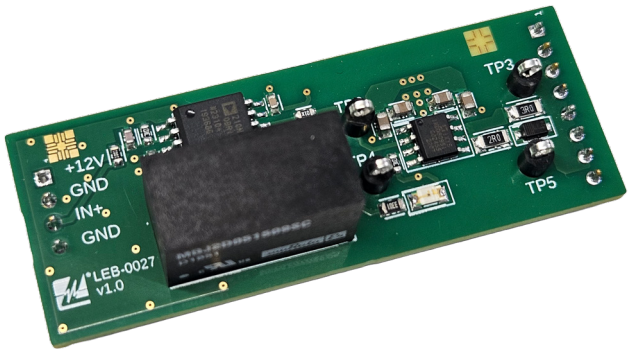

Figure 1. IXDD609SI gate driver evaluation board

The evaluation board is part of the Littelfuse gate driver evaluation platform for testing gate drivers with various power semiconductors. Pin headers enable easy integration into existing test setups. Additionally, the platform contains different mainboards, that allow immediate testing and comparison of Littelfuse gate drivers with various power semiconductors. All parts are available from Littelfuse upon request.

Features

Device IXDD609SI:

- 9 A peak source/sink output
- Matched rise and fall times
- Low propagation delay time
- Low, 10 µA supply current
- Low output impedance
- Wide operating voltage range: 4.5 V to 35 V
- Temperature range of -40 °C to +125 °C
- Logic input withstands negative swing of up to 5 V

Evaluation Board:

- Single primary side 12 V power supply
- Isolated DC-DC converter with +15 V/-9 output voltage
- On-board gate resistors
- 5000 V_{RMS} – rated digital isolator
- Defined creepage of 5.5 mm between primary and secondary circuit

Target Audience

This user manual is intended for engineers working on power electronics hardware design and investigating optimal driver solutions for their applications.

Contact Information

For more information on the evaluation board and application support, contact the Littelfuse Power Semiconductor team of product and applications experts: PowerSemiSupport@Littelfuse.com

Revised: TK.04/30/2025

Important Notes

Disclaimer Notice: The Customer (individually or, if you are acting on behalf of a company, the company) agrees to use the Evaluation Board solely for this purpose and subject to the terms of this Notice.

The design of the Evaluation Board has been tested by Littelfuse only as described in this document. The design is not qualified in terms of safety requirements, manufacturing, and operation over the entire operating temperature range or lifetime.

The Evaluation Board is an engineering tool intended solely for laboratory use by qualified and experienced electrical engineers to evaluate the performance of Littelfuse power semiconductors and integrated circuit products according to the terms and conditions set forth in this document or other related documents supplied with the respective Evaluation Board. The Evaluation Board should not be used at all or as part of a finished product.

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1. Overview

The block diagram of the evaluation board is depicted in Figure 2. It contains an isolated DCDC-Converter MGJ2D121509SC from Murata Power Solutions (U2) providing isolated +15/-9 V gate driver supply on the secondary side. On the primary and secondary sides, two 5 V regulators (U1, U3) supply the ADuM210N signal isolator (U4). The output signal of the signal isolator serves as input signal for the IXDD609SI driver IC (U5), which delivers sink and source output currents of up to 9 A to the power semiconductor's gate.

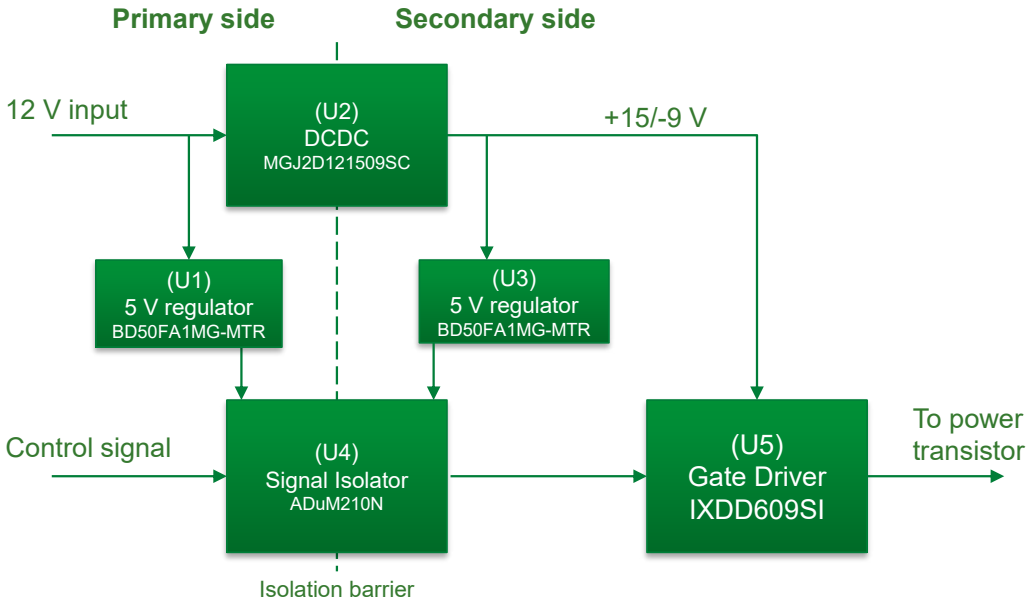

Figure 2. IXDD609SI evaluation board block diagram

Table 1 contains the operating conditions of the evaluation board.

Table 1. Operating conditions of the IXDD609SI evaluation board

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
V_{CC}	Board supply voltage	11	12	13	V
$V_{Control}$	Control signal input voltage	–	5	5.5	V
V_{IH}	Control signal input voltage high threshold	–	3.5	–	V
V_{IL}	Control signal input voltage low threshold	–	1.5	–	V
I_{OUTSRC}, I_{OUTSNK}	Output peak current	–	–	±9	A
$I_{OUTSOFT}$	Soft turn off peak current	–	–	1	A
dv/dt	Voltage change rate secondary to primary side(1)	–	–	75	V/ns
d_{Creep}	Creepage distance primary to secondary side	–	5.5	–	mm
d_{Creep}	Clearance distance primary to secondary side	–	5.5	–	mm
T_{AMB}	Operation ambient temperature	0	25	50	°C

Note:
(1) Based on digital isolator ADuM210N datasheet values

2. Pin Assignments

Table 2 describes the electrical connections of the evaluation board. A 4-terminal pin header is used to connect the PCB on the primary side. On the secondary side, the evaluation board is connected via an 8-terminal pin header. Additionally, four test points are available to record driver signals during operation.

Table 2. Pin assignments of the IXDD609SI evaluation board

Connector Name	Pin Number	Pin Name	Description
X1	01	+12 V	Positive 12 V supply primary side
X1	02	GND	Primary side reference
X1	03	IN_+	Driver input signal
X1	04	GND	Primary side reference
X2	01	RES	Reserved pin
X2	02	VEE_HV	Gate-loop return path
X2	03	OUT_GATE	Gate output
X2	04	VEE_HV	Gate-loop return path
X2	05	OUT_GATE	Gate output
X2	06	VEE_HV	Gate-loop return path
X2	07	OUT_GATE	Gate output
X2	08	RES	Reserved pin
–	–	TP1	IXDD609SI input signal test point
–	–	TP2	Gate connection test point
–	–	TP3	XDD609SI enable test point
–	–	TP4	Gate-loop return path test point

3. Schematics

Figure 3 illustrates the evaluation board's schematic. The upper part of the circuit shows the isolated power supply of the board. The MGJ2D121509SC DC-DC converter provides isolated driver supply of +15/-9 V. If a unipolar supply is needed, for example to drive silicon MOSFETs, the resistor R2 can be removed and a 0 Ω jumper R1 must be added. LED1 indicates the presence of the +15 V gate driver supply voltage.

The lower part of the schematic depicts the signal isolator and the IXDD609SI driver stage. A low-pass filter is connected to the input side of the signal isolator. Depending on the power semiconductor in use and the required gate current, the gate resistors for turn-on and turn-off can be adjusted. Testpoints on the PCB allow measurement of driver inputs and outputs.

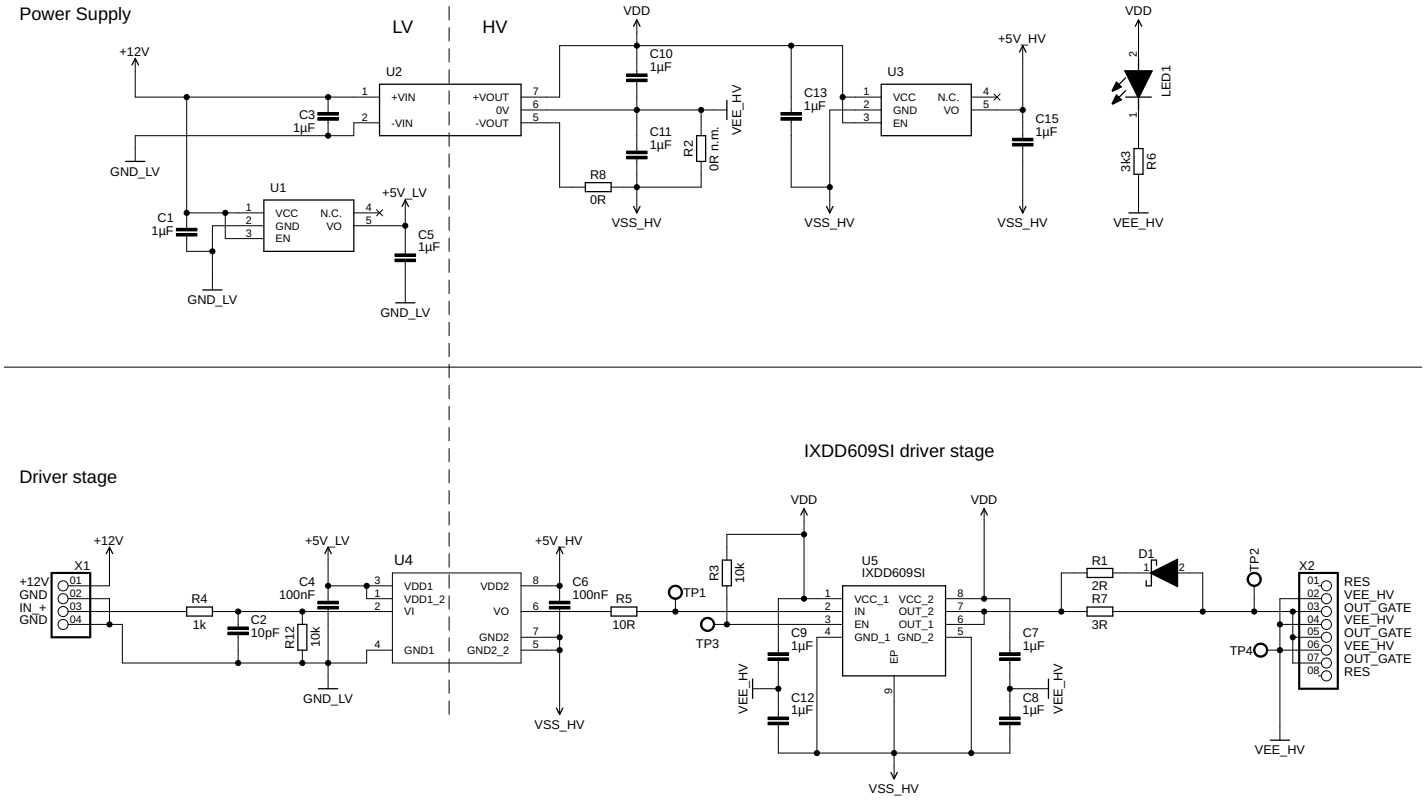

Figure 3. IXDD609SI evaluation board schematics

4. Bill of Materials

Table 3 lists all the components used on the evaluation board.

Table 3. Bill of materials for the IXDD609SI evaluation board

Item	Quantity	Reference	Value	Description	Manufacturer	MPN
1	2	C4, C6	100 nF	Cap 100 nF 25 V 10 % X7R 0603	-generic-	–
2	1	C2	10 pF	Cap 10 pF 25 V 10 % C0G 0603	-generic-	–
3	11	C1, C3, C5, C7, C8, C9, C10, C11, C12, C13, C15	1 µF	Cap 1 µF 50 V 10 % X7R 0805	-generic-	–
4	2	R2, R8	0 Ω	Jumper 0 Ω 0805	-generic-	–
5	1	R5	10 Ω	Res 10 Ω 10 % 0603	-generic-	–
6	2	R3, R12	10 kΩ	Res 10 kΩ 10 % 0603	-generic-	–
7	1	R4	1 kΩ	Res 1 kΩ 10 % 0603	-generic-	–
8	1	R1	2 Ω	Res 2 Ω 1 % 1206	-generic-	–
9	1	R7	3 Ω	Res 3 Ω 1 % 1206	-generic-	–
10	1	R6	3.3 kΩ	Res 3.3 kΩ 10 % 0805	-generic-	–
11	1	LED1	–	LED green 1206	Wuerth Elektronik	150120VS75000
12	1	U4	–	Digital isolator 5 kV	Analog Devices	ADUM210N0BRIZ
13	2	U1, U3	–	LDO Voltage Regulators 5 V/0.1 A	ROHM Semiconductor	BD50FA1MGMTR
14	1	U5	–	9 A Low side gate driver	Littelfuse	IXDD609SI
15	1	U2	–	Isolated DC-DC 12 V to +15/-9 V	Murata Power Solutions	MGJ2D121509SC
16	1	D1	–	Schottky Diode 40 V/3 A	Nexperia	PMEG4030ETRX
17	1	X1	–	Pin header 0.1" pitch 4-pin	Samtec	HTSW-104-05-G-S
18	1	X2	–	Pin header 0.1" pitch 8-pin	Samtec	HTSW-108-05-G-S
19	4	TP1, TP2, TP3, TP4	–	Testpoint THT	Keystone	5006

5. Isolation Ratings

The isolation between the primary and secondary sides of the circuit is provided by the DC- DC converter U2 and the digital isolator U4. The DC-DC converter provides high voltage isolation of up to 5200 V_{DC} with an isolation capacitance of 4 pF. The ADUM210N0 digital isolator provides high voltage isolation of up to 5000 V_{RMS} with an isolation capacitance of 2 pF. For further details on isolation capability of the devices, refer to the MGJ2D121509SC and ADUM210N0 datasheets.

The creepage and clearance distances on the PCB between the primary and secondary side are 5.5 mm.

6. PCB Layout

Figures 4 to 7 display the four copper layers of the PCB.

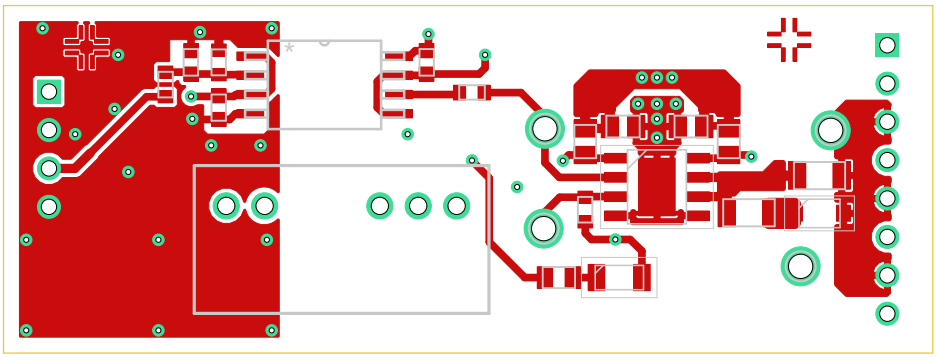

Figure 4. PCB top layer

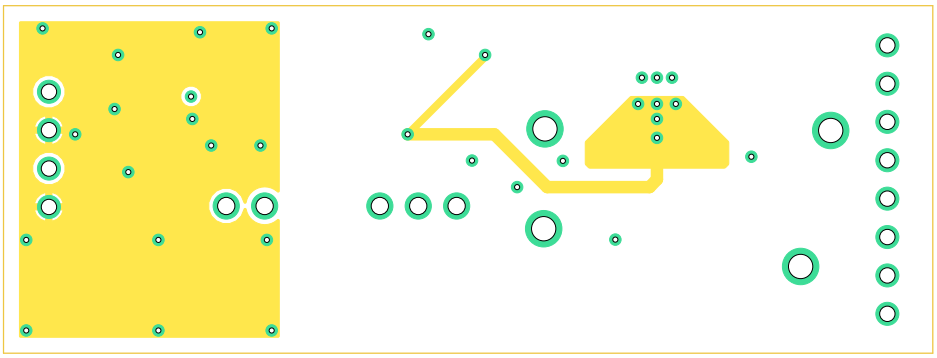

Figure 5. PCB layer 2

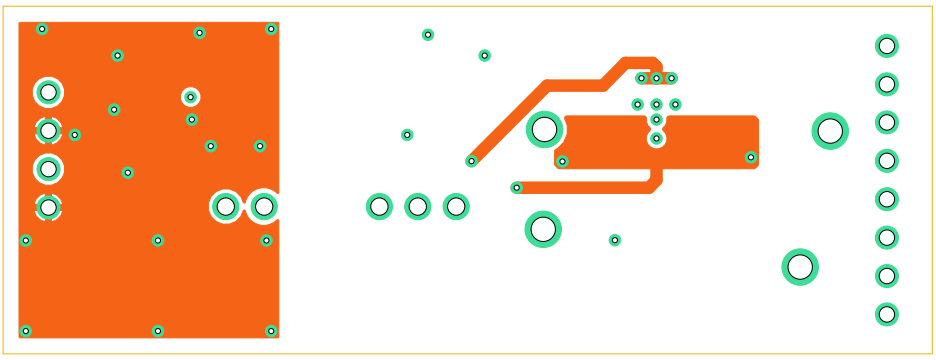

Figure 6. PCB layer 3

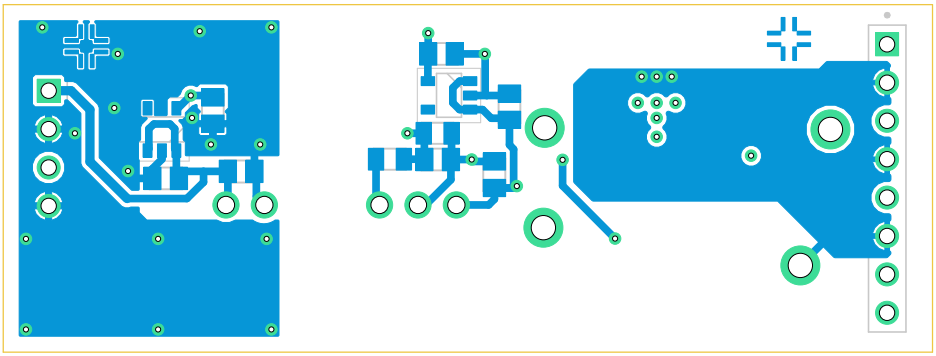

Figure 7. PCB bottom layer

7. PCB Assembly Data

Figure 8 and Figure 9 show the PCB assembly, including the mechanical dimensions of the evaluation board in millimeters.

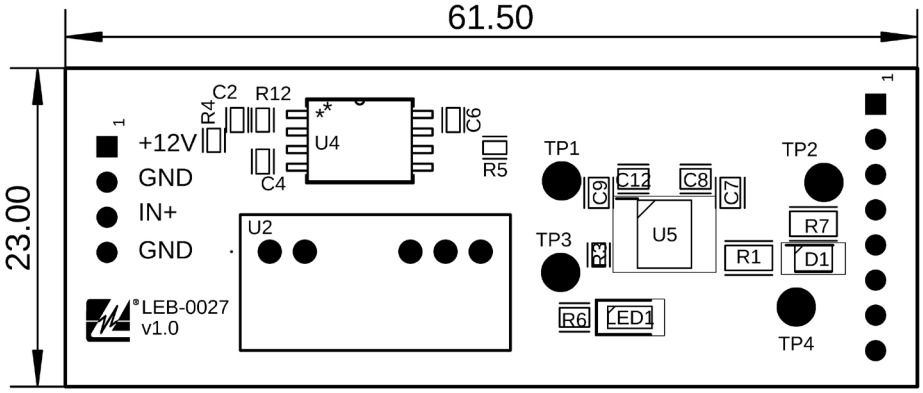

Figure 8. PCB top assembly and dimensions

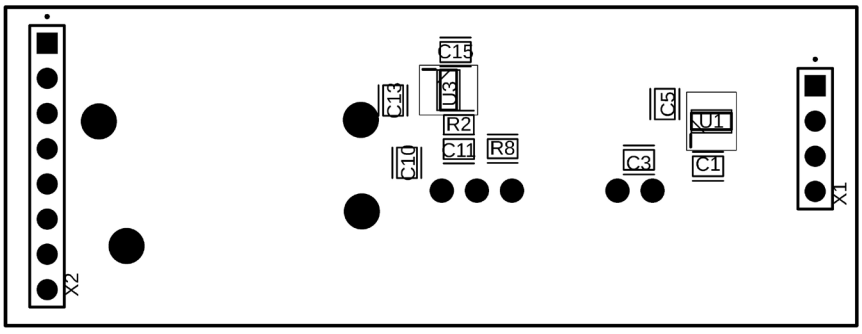

Figure 9. PCB bottom assembly (mirrored view)

Revision History

Date	Revision	Changes
April 2025	1.0	Initial Release