LEB-0034
Gate Driver Evaluation Mainboard for TOLL Packages

Introduction

Littelfuse offers a broad range of power semiconductor gate drivers with various features. These include both isolated and non-isolated drivers of different current classes, as well as drivers that incorporate safety features such as desaturation detection, soft turn-off, and fault state feedback. A gate driver evaluation platform has been introduced to enable customers to evaluate the gate driver portfolio under comparable conditions. This platform includes multiple gate driver boards that are compatible with mainboards designed for different power semiconductor packages. This manual describes the platform's mainboard for TOLL packages. It allows testing of various combinations of gate drivers and power transistors within the same setup. The mainboard can be equipped with different gate driver evaluation boards and various power transistors in TOLL packages.

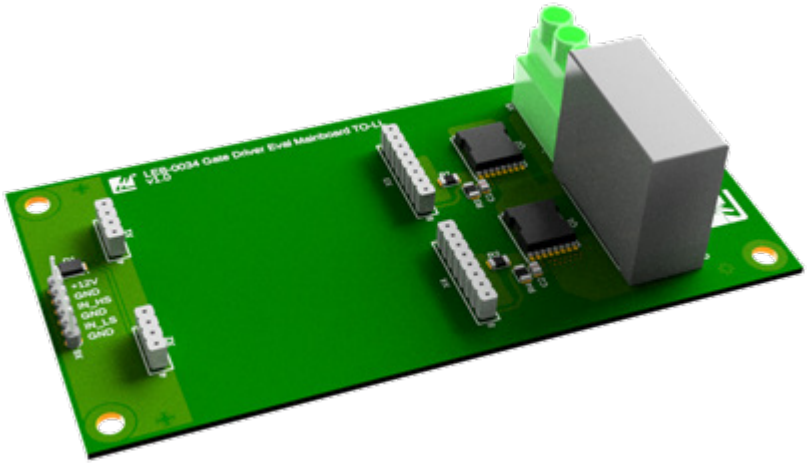

Figure 1. Littelfuse gate driver evaluation platform mainboard for TOLL packages

Features

- Ability to test and compare different Littelfuse gate driver solutions with power semiconductors in TOLL packages
- Maximum operating voltage: 500 V
- Suitable for double pulse and application-related testing

Target Audience

This manual is intended for engineers working on power electronics hardware design and investigating optimal gate driver and power semiconductor solutions for their applications.

Contact Information

For more information on the evaluation board and application support, contact the Littelfuse Power Semiconductor team of product and applications experts: PowerSemiSupport@Littelfuse.com

Important Notes

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The design of the Evaluation Board has been tested by Littelfuse only as described in this document. The design is not qualified in terms of safety requirements, manufacturing and operation over the entire operating temperature range or lifetime.

The Evaluation Board is an engineering tool intended solely for laboratory use by qualified and experienced electrical engineers to evaluate the performance of Littelfuse power semiconductors and integrated circuit products according to the terms and conditions set forth in this document or other related documents supplied with the respective Evaluation Board. The Evaluation Board should not be used at all or as part of a finished product.

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Table of Contents

List of Figures

1. Overview

Figure 2 displays the block diagram and top view of the gate driver evaluation mainboard for TOLL packages. The board can be used for standard double pulse tests if it is not attached to a heatsink. For continuous operation, the board must be attached to a heatsink by using an electrically isolating thermal interface material. The desired driver evaluation boards are plugged onto the connectors X1 and X3 for high side connection, and connectors X2 and X4 for low side connection for testing purposes. The supply voltage and the control signals are provided through connector X6. Terminal block X5 is used for connecting the DC-Link voltage and auxiliary components, such as a choke or a resistor for double-pulse tests.

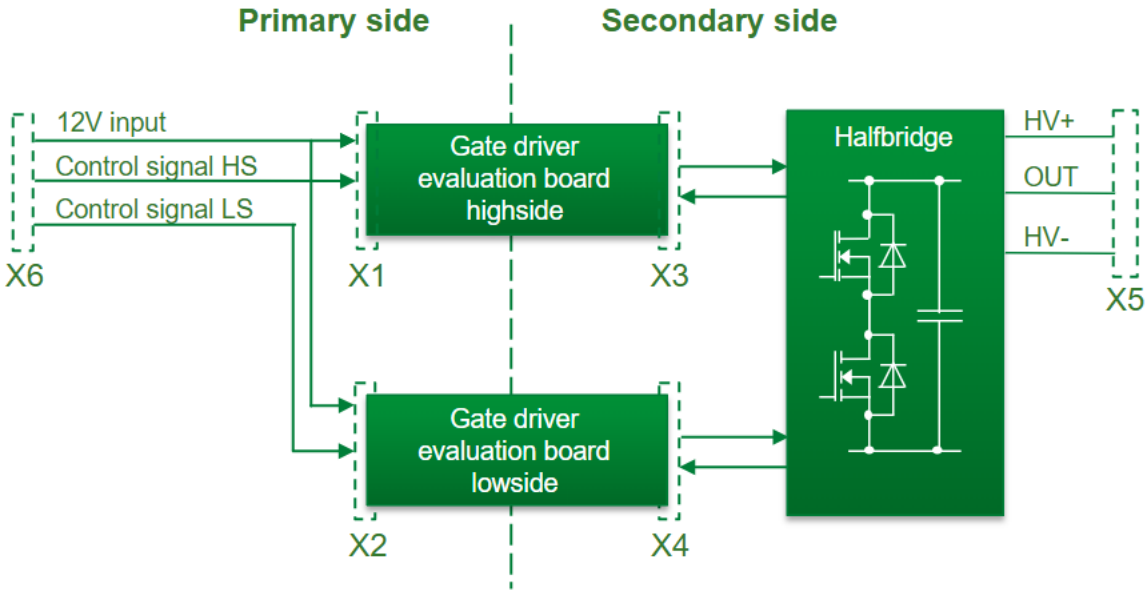

Figure 2. Gate driver evaluation mainboard block diagram

Table 1 contains the operating conditions of the driver evaluation mainboard.

Table 1. Operating conditions of the gate driver evaluation mainboard

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
V_{CC}	Board primary side supply voltage	11	12	13	V
$U_{control}$	Primary side control signal input voltage	–	5	5.5	V
U_{HV}	Secondary side operating voltage(1)	–	–	500	V
I_{HV}	Secondary side load current(2)	–	–	50	A
T_{amb}	Operating ambient temperature	0	25	50	°C

Notes:
(1) See Section 5 for further details on isolation ratings.
(2) Operation in double pulse test. Not for continuous operation.

Please be aware that depending on the power semiconductor in use, the gate driver voltages on the driver evaluation boards must be adjusted accordingly. In standard configuration, the driver evaluation boards are equipped with power supply of +15/-9 V.

2. Pin Assignments

Table 2 describes the electrical connections of the mainboard. A 4-terminal socket strip is used to connect the gate driver evaluation boards on the primary side. On secondary side, the evaluation boards are connected via an 8-terminal socket strip. The power circuit is connected via a 3-pole terminal block.

Table 2. LEB-0034 pin assignments

Connector Name	Pin Number	Pin Name	Description
X1	1	+12 V	+12 V supply high-side gate driver
X1	2	GND	Primary-side GND
X1	3	IN+	PWM input high-side gate driver
X1	4	GND	Primary-side GND
X2	1	+12 V	+12 V supply low-side gate driver
X2	2	GND	Primary-side GND
X2	3	IN+	PWM input low-side gate driver
X2	4	GND	Primary-side GND
X3	1	DESAT_FB	High-side desaturation detection feedback pin (reserved for IX4352NE)
X3	2	SOURCE_EMITTER	High-side power transistor source/emitter connection
X3	3	DRIV_OUT	High-side gate driver evaluation board gate output
X3	4	SOURCE_EMITTER	High-side power transistor source/emitter connection
X3	5	DRIV_OUT	High-side gate driver evaluation board gate output
X3	6	SOURCE_EMITTER	High-side power transistor source/emitter connection
X3	7	DRIV_OUT	High-side gate driver evaluation board gate output
X3	8	GATE_FB	High-side gate feedback pin (reserved for IX4352NE)
X4	1	DESAT_FB	Low-side desaturation detection feedback pin (reserved for IX4352NE)
X4	2	SOURCE_EMITTER	Low-side power transistor source/emitter connection
X4	3	DRIV_OUT	Low-side gate driver evaluation board gate output
X4	4	SOURCE_EMITTER	Low-side power transistor source/emitter connection
X4	5	DRIV_OUT	Low-side gate driver evaluation board gate output
X4	6	SOURCE_EMITTER	Low-side power transistor source/emitter connection
X4	7	DRIV_OUT	Low-side gate driver evaluation board gate output
X4	8	GATE_FB	Low-side gate feedback pin (reserved for IX4352NE)
X5	1	HV+	Load circuit positive terminal
X5	2	HV-	Load circuit negative terminal
X5	3	OUT	Half-bridge output terminal
X6	1	+12V_LV	+12 V board supply
X6	2	GND_LV	Primary-side GND
X6	3	IN+_HS	High-side driver PWM input
X6	4	GND_LV	Primary-side GND
X6	5	IN+_LS	Low-side driver PWM input
X6	6	GND_LV	Primary-side GND

3. Schematics

The mainboard's schematic is depicted in Figure 3. On the left side, the driver control signals and the 12 V power supply are routed directly from connector X6 to the connectors X1 and X2 of the evaluation boards. The 12 V power supply line is equipped with reverse polarity protection. The right side of the schematic shows the power semiconductor circuitry on the mainboard. The Littelfuse MOSFETs in TOLL packages are connected in a half-bridge configuration, connected to a DC-Link with passive discharge resistors.

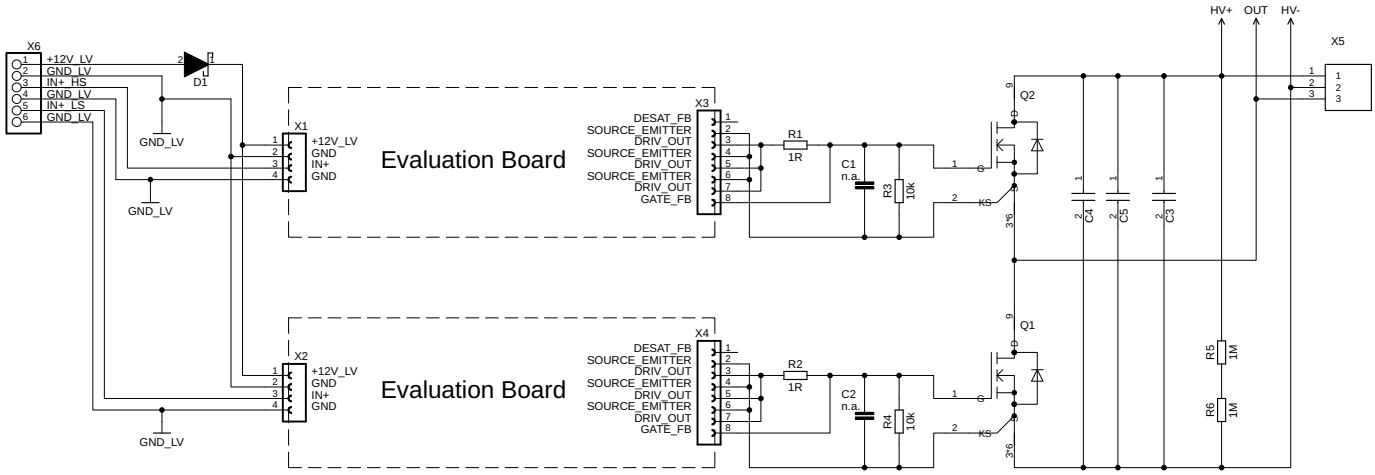

Figure 3. TOLL mainboard schematics

4. Bill of Materials

Table 3 contains the evaluation board's bill of materials.

Table 3. Bill of materials for the gate driver evaluation mainboard

Item	Quantity	Reference	Value	Description	Manufacturer	MPN
1	1	C3	7 µF	Film Cap 700 V 7 µF 5 %	Kemet	C4AQJBU4700M1YJ
2	2	C4, C5	0.22 µF	MLCC X7R 2220 630 V 0.22µF	Kemet	C2220X224KBRACTU
3	2	R1, R2	1 Ω	Res 1 Ω 1 % 1206	- generic -	–
4	2	R3, R4	10 kΩ	Res 10 kΩ 10 % 1206	- generic -	–
5	2	R5, R6	1 MΩ	Res 1 MΩ 3kV 5 % 2512	- generic -	–
6	1	D1	–	1 A low V_F Schottky barrier rectifier	Nexperia	PMEG6010EP, 115
7	2	Q1, Q2	–	MOSFET TOLL-package	Littelfuse	–
8	2	X1, X2	–	.100" Closed Entry Low Profile Socket Strip	SAMTEC	CES-104-01-T-S
9	2	X3, X4	–	.100" Closed Entry Low Profile Socket Strip	SAMTEC	CES-108-01-T-S
10	1	X5	–	Fixed Terminal Block 3P 6.35 mm 90°	Phoenix Contact	1714968
11	1	X6	–	Pin header 0.1" pitch 6-pin	SAMTEC	TSW-106-23-H-S

5. Isolation Ratings

The creepage distances between primary- and secondary- side on the mainboard are very large. The isolation capability between primary- and secondary-side of the overall setup is therefore given by the isolation capability of the gate driver evaluation board, which is mounted on the mainboard. Refer to the user manual of the respective driver evaluation board.

The board is specified for a maximum operating voltage of 500 V. In accordance with the IEC 60664-1 standard, the assumption of pollution degree 2 and material group 1 of the PCB-material, the required creepage distances for 500 V operating voltage are 2.5 mm.

6. PCB Layout

Figures 4 to 7 display the four copper layers of the PCB.

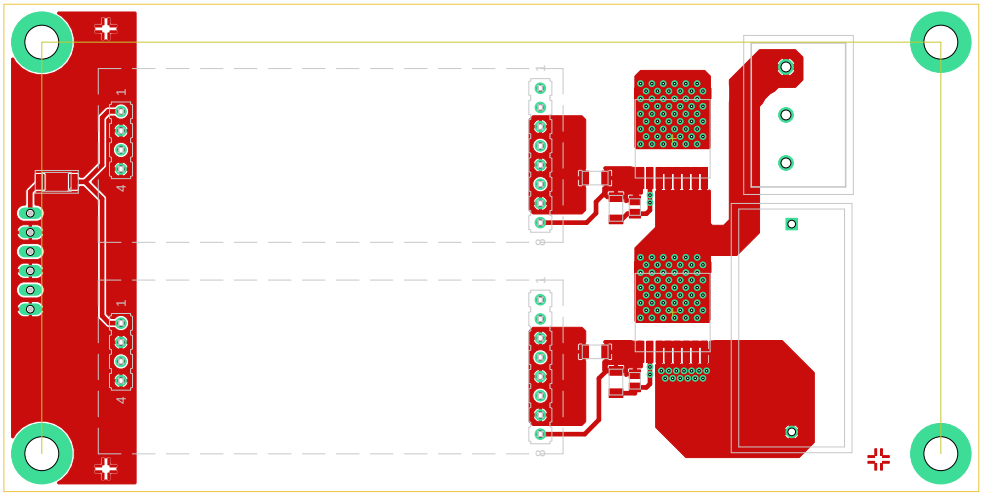

Figure 4. PCB top layer

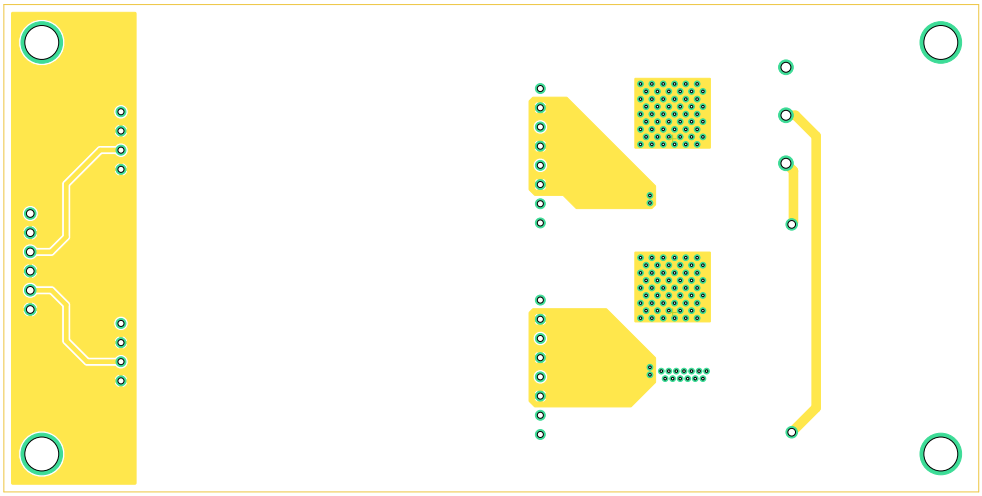

Figure 5. PCB layer 2

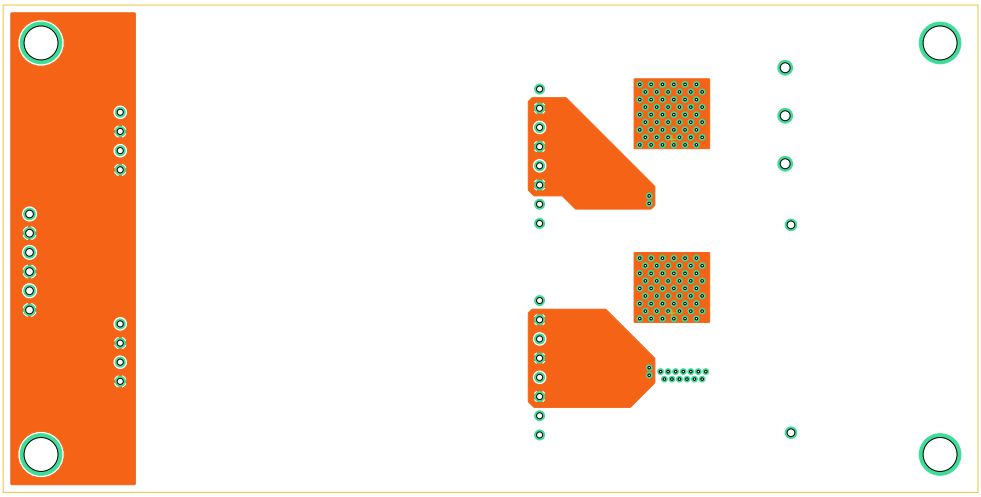

Figure 6. PCB layer 3

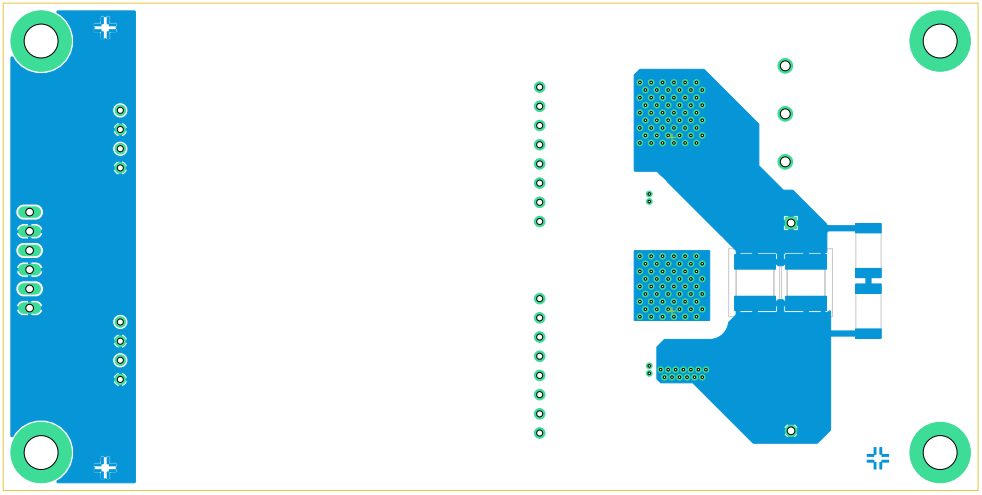

Figure 7. PCB bottom layer

7. PCB Assembly Data

Figure 8 and Figure 9 depict the PCB assembly, including the mechanical dimensions of the mainboard.

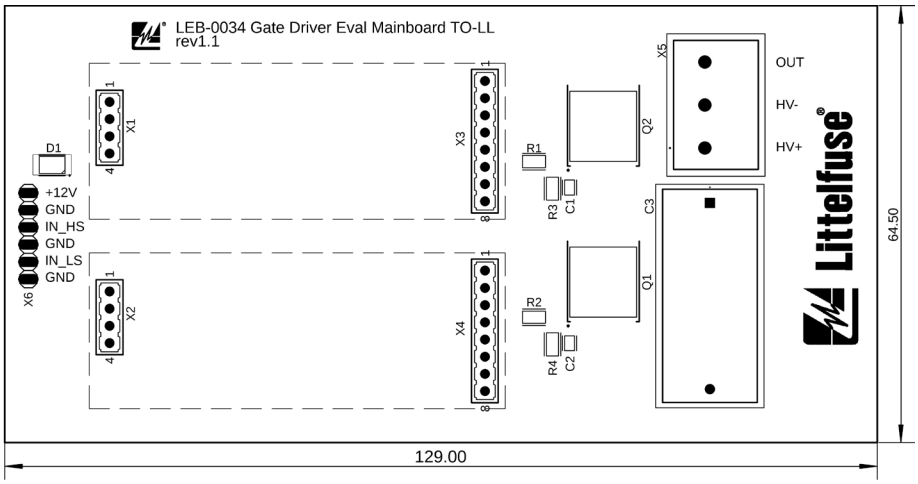

Figure 8. PCB top assembly and dimensions

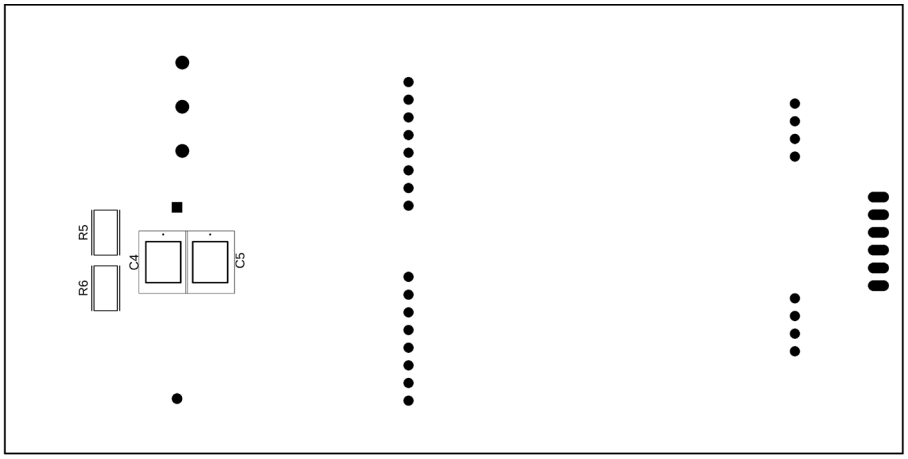

Figure 9. PCB bottom assembly

Revision History

Date	Revision	Changes
April 2025	1.0	Initial Release