

# **Designing Surge and Power Fault Protection Circuits for Solid State Subscriber Line Interfaces**

## Contents

|     |                                                                |    |
|-----|----------------------------------------------------------------|----|
| 1   | Introduction .....                                             | 4  |
| 1.1 | The Fully Solid State Subscriber Line Interface .....          | 4  |
| 1.2 | The Requirement for Surge and Power Fault Protection .....     | 5  |
| 2   | Lightning Surge and AC Power Fault Testing .....               | 5  |
| 2.1 | Commonly Referenced Regulatory Requirements .....              | 5  |
| 2.2 | Testing Methods .....                                          | 6  |
| 3   | Design of Protection .....                                     | 9  |
| 3.1 | Protection Strategies .....                                    | 9  |
| 3.2 | Design Examples for Protected Solid State Line Interface ..... | 12 |
| 3.3 | Other Considerations .....                                     | 18 |
| 4   | Appendix .....                                                 | 20 |
| 4.1 | The Energy Transferred by a Lightning Surge. ....              | 20 |
| 4.2 | Power Dissipation During an AC Power Fault. ....               | 22 |
| 4.3 | Telecommunications Protection Rated Component Sources .....    | 28 |
| 5   | References .....                                               | 30 |

## Figures

|           |                                                                             |    |
|-----------|-----------------------------------------------------------------------------|----|
| Figure 1  | Solid State Subscriber Interface .....                                      | 4  |
| Figure 2  | Lightning Surge Induction .....                                             | 5  |
| Figure 3  | Double Exponential Lightning Waveform .....                                 | 7  |
| Figure 4  | Levels of Protection .....                                                  | 7  |
| Figure 5  | Basic Test Connection Methods .....                                         | 8  |
| Figure 6  | Current Steering Example .....                                              | 11 |
| Figure 7  | Tertiary Protection Components Provided by the LCAS .....                   | 12 |
| Figure 8  | Reference Design .....                                                      | 14 |
| Figure 9  | Example Secondary Protection Circuit Solutions .....                        | 17 |
| Figure 10 | Ground Bounce Measurement .....                                             | 18 |
| Figure 11 | Approximation of the 10 x 1000 $\mu$ s, Double Exponential Waveform .....   | 20 |
| Figure 12 | Back to Back Zener Over Voltage Protector Operation .....                   | 23 |
| Figure 13 | Crowbar Type Over Voltage Protector Operation – Asymmetric Thresholds ..... | 26 |

## Tables

|         |                                                                         |    |
|---------|-------------------------------------------------------------------------|----|
| Table 1 | Test Severity Terminology and Pass Criteria .....                       | 8  |
| Table 2 | Test Generator Output Resistance .....                                  | 10 |
| Table 3 | Current Consumption versus Operating State .....                        | 13 |
| Table 4 | Less Appropriate Protection Component Types .....                       | 16 |
| Table 5 | Secondary Protection Parts Lists .....                                  | 17 |
| Table 6 | Lightning Surge Energy Examples– 10 x 1000 $\mu$ s, 1000 V, 100 A ..... | 22 |

## Abstract:

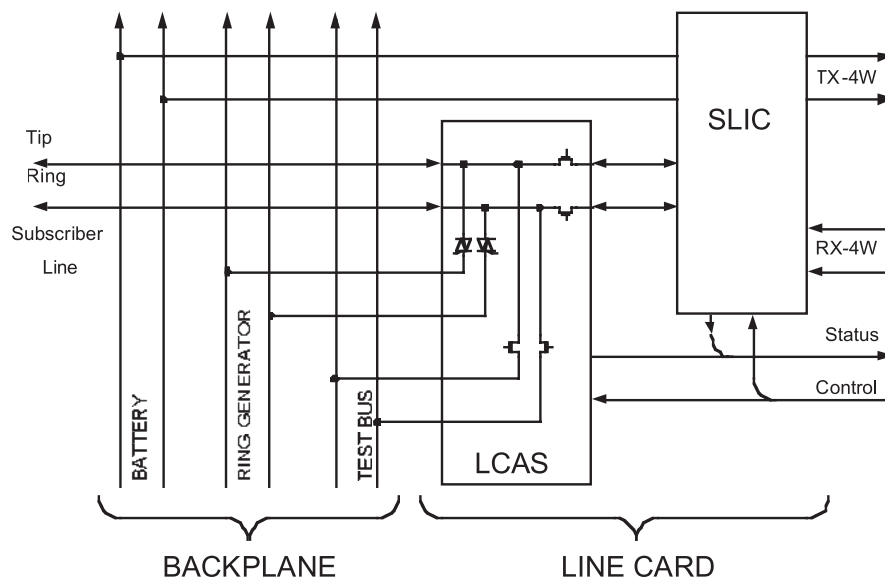
This application note is intended to assist the user of solid state Subscriber Line Interface Circuit (SLIC) and Line Card Access Switch (LCAS) devices in meeting the stringent requirements of lightning surge and AC power fault testing. As telecommunication equipment designers respond to market demand for increased line card functionality at reduced cost, they continue to rely ever more heavily on application specific solid state circuit solutions. These solutions now address even the subscriber line interface and line access arrangements, an environmentally harsh domain formerly dominated by bulky transformers and electromechanical relays. Robust design with these new integrated circuits requires a good understanding of the methods used by the regulatory bodies to verify product durability and safety and the knowledge to select the external surge protection components that coordinate effectively with the safety features already designed into these integrated subscriber interface devices. Background on surge protection compliance testing is provided, protection methodologies are developed and example designs presented.

## 1 INTRODUCTION

Escalating subscriber demand for expanded telecommunication services continues to strain the capacity of the PSTN infrastructure. Additionally, competing technologies are exerting downward price pressure on the operating companies. Both of these trends have required telecommunications hardware manufacturers to pursue increased channel density at reduced per channel cost. Not surprisingly, increased utilization of solid state semiconductor components has helped to achieve these objectives. Successful application of these newer technologies requires a good understanding of the rigors of lightning and power fault testing.

### 1.1 The Fully Solid State Subscriber Line Interface

More designers of network and customer premises equipment have been taking advantage of opportunities to replace magnetic and electromagnetic components with solid state devices to obtain reduced size, weight and cost and to reduce the heat loads in equipment shelves that go hand in hand with increased circuit density. As one clear indicator of this evolution, the solid state Subscriber Loop Interface Circuit (SLIC) has become a widely accepted alternative to the transformer based 4-wire to 2-wire hybrid interface and associated discrete battery feed electronics. More recently, the integrated solid state Line Card Access Switch (LCAS) has seen increasing application as designers have learned how to use it to replace traditional electromechanical relays, or even clusters of discrete solid state relays, in subscriber line switching circuits. *Figure 1* illustrates an example of a single channel access arrangement.

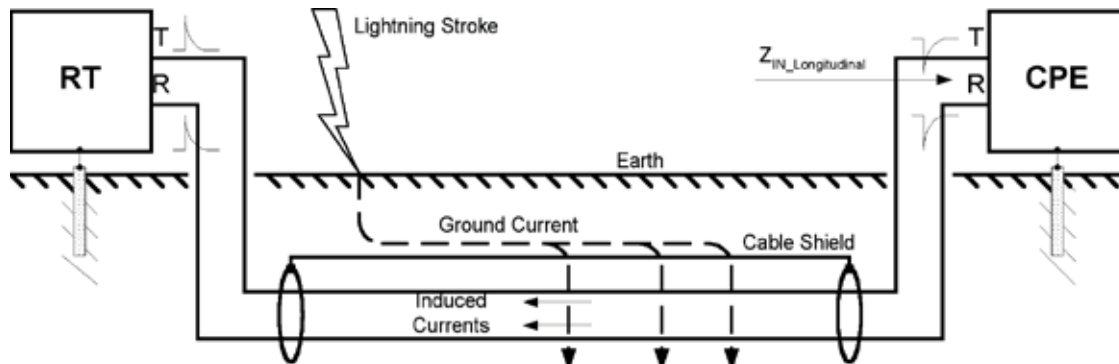


**Figure 1 Solid State Subscriber Interface**

As is so often the case in semiconductor technology, an integrated circuit alternative to older technologies can bring additional benefits or features to the application. In this case, the LCAS allows a simple logic level control interface with the embedded processor. Perhaps more importantly, however, the LCAS device is equipped to provide substantial additional surge protection and line fault isolation for the SLIC.

## 1.2 The Requirement for Surge and Power Fault Protection

It is well understood that the outside cable plant of the PSTN is subject to a wide variety of severe electrical disturbances. The sources of the most damaging disturbances are generally either lightning discharges or AC power lines. Electrical current from either type of source may gain access to telecommunication cabling by direct contact and conduction or by magnetic induction. As one example, *Figure 2* represents the ground current flow mechanism by which a lightning surge may be induced into a subscriber loop. If the cable shield happens to enhance current flow during the lightning event, as might especially occur in an aerial installation, the induction effect may be greatly increased.



**Figure 2 Lightning Surge Induction**

Most disturbances due to lightning as well as many lower level AC power disturbances are coupled into the network by magnetic induction. This leads to the interesting observation that most surges appearing at the equipment terminals are common mode in nature since the surge current polarity will be the same in both the Tip and the Ring conductors. Differential mode surges can be caused by direct contact but are much more commonly the result of unbalanced operation of surge protection devices on the line. Unbalanced current flow to earth ground through those devices then produces large voltage differences between conductors in the pair.

## 2 LIGHTNING SURGE AND AC POWER FAULT TESTING

The product development schedule must contain *ample* time for testing. The budget for compliance verification testing can represent more than a third of the entire cost of development. Pre-qualification testing is almost indispensable since failures or design modifications during formal compliance testing are very costly in terms of project expense and product release schedule.

The world's telecommunications regulatory and standards bodies have gathered extensive field data aimed at quantifying the nature and severity of lightning surges and interference from AC power lines in order to establish qualification testing requirements for exposed equipment. For instance, Bellcore document TR-EOP-000001<sup>1</sup> used data collected at Central Office facilities in Washington, CT, Cleveland, SC, and Kentwood, LA, to establish the lightning test waveforms embodied in the lightning surge test requirements of Telcordia Technologies<sup>2</sup> (Bellcore) GR-1089-CORE<sup>3</sup>, the primary electromagnetic compatibility and safety standard for the PSTN in North America.

### 2.1 Commonly Referenced Regulatory Requirements

European and some Asian markets require that the equipment withstand the surge and power fault test requirements established by the Telecommunication Standardization Sector of the International Telecommunication Union. Document ITU-T K.20<sup>4</sup> covers telephone exchanges and switching centers. Document ITU-T K.21<sup>5</sup> covers desk-borne equipment and other sorts of customer premises devices. The ITU-T (formerly CCITT) documents are based

<sup>1</sup> Bellcore TR-EOP-000001, Issue 2, June 1987, *Lightning, Radio Frequency and 60 Hz Disturbances at the Bell Network Interface*.

<sup>2</sup> Bellcore was jointly owned and operated by the RBOCs since the breakup of the old AT&T/Bell system in 1984. As competition among the RBOCs gradually escalated since that time, they found it increasingly awkward to engage in the cooperative research necessary to keep Bellcore at the forefront of technological development. In late 1997, the operating companies sold Bellcore to Science Applications International Corp (SAIC) who then renamed the organization Telcordia Technologies.

<sup>3</sup> Telcordia (Bellcore) GR-1089-CORE, Issue 2, December 1997, Rev 1, February 1999: *Electromagnetic Compatibility & Electrical Safety - Generic Criteria for Network Communications*.

<sup>4</sup> ITU-T (CCITT), K.20, 10/96, Protection Against Interference; *Resistibility of Telecommunication Switching Equipment to Overvoltages and Overcurrents*.

<sup>5</sup> ITU-T (CCITT), K.21, 10/96, Protection Against Interference; *Resistibility of Subscriber's Terminal to Overvoltages and Overcurrents*.

on CCITT recommendations dating from 1988 carrying the same K-series numbers. Guidelines which help determine the appropriate test environment for a given item of equipment are found in ITU-T K.11<sup>1</sup> although the final determination is under the authority of the test administrator.

In North America, lightning surge and AC power fault withstand requirements are set forth by Telcordia in Section 4 of GR-1089. Other sections of that document cover electromagnetic compatibility and safety. In the Telcordia (Bellcore) hierarchy of standards, this Generic Requirements (GR) document is incorporated as a module into such wide-scope Telcordia standards as the LSSGR<sup>2</sup> and NEBSFR<sup>3</sup>. Compliance with GR-1089 or, more generally, "NEBS" is typically specified in the RFPs and equipment purchase orders of the North American RBOCs (Regional Bell Operating Companies), or, more appropriately these days, the ILECs (Incumbent Local Exchange Carriers) and is, consequently, the most widely adhered to standard by vendors in that market. The CLECs or Competitive Local Exchange Carriers are generally obliged to adhere to these same NEBS standards as a precondition to installing access equipment into or integrating it with an existing ILEC facility. NEBS compliance also presumably offers an effective liability shield.

Other standards apply to telecommunications customer premise equipment (CPE). In the U.S., the Federal Communications Commission (FCC) has incorporated certain standards for terminal equipment connected to the PSTN into U.S. law. These are contained in Part 68<sup>4</sup> of Title 47 of the Code of Federal Regulations (CFR). Part 68 details many of the characteristics of such terminal equipment including, for example, the precise mechanical specifications for the ubiquitous modular phone plugs and jacks. Of interest in the present context, there are lightning surge withstand requirements to be found in paragraph 68.302. These lightning and voltage withstand requirements are less severe than those of GR-1089. It is also worth noting in passing that since surge protection circuits have the potential for affecting parameters such as the impedance of the line connection or the leakage currents, the designer may need to consider other paragraphs of Part 68 also. In a related item, it should be mentioned that under the North American trade treaty known as NAFTA, Part 68 and its Canadian counterpart (CS-03) have been harmonized while the governing Mexican regulation (NOM-EM-151-SCT1-1997) remains substantially different as of this writing.

On the safety side, the National Electrical Code<sup>5</sup> (NEC) requires that all customer premise equipment be listed by a Nationally Recognized Laboratory (NRL) such as Underwriters Laboratories Inc. (UL). This has traditionally meant satisfying the requirements of UL 1459 and one or more parts of the UL 497 series (which is primarily concerned with the fire hazard aspects, e.g. construction materials of surge protection devices). As part of the trend toward global harmony among national standards, UL 1459 is in the process of being supplanted by UL 1950 / CSA C22.2 No. 950-95 which merges the requirements of the UL and Canadian standards. As of 1 April, 2000, all newly marketed affected products will be evaluated against the updated standard. As of 5 April, 2005, listings under the old UL 1459 standard will no longer be recognized. Old product designs must then be demonstrated to comply with UL 1950. (The low marketability of old technology equipment will probably render such re-certification cost ineffective in most cases.) This change also moves the North American safety standards closer to the European safety requirements contained in IEC 60950<sup>6</sup> (formerly IEC 950).

## 2.2 Testing Methods

Lightning tests consist of discharging a known stored quantity of energy into the Equipment Under Test (E.U.T.) through a specified impedance. The voltage and/or current waveforms are exponential in nature and are specified either by defining the surge generator's output equivalent circuit or by defining the generator as a black box with a given open circuit voltage waveform and a given short circuit current waveform. GR-1089 uses the latter method; the ITU-T provides equivalent circuit diagrams for the generators. A number of companies manufacture specialized generating equipment capable of producing the various required surge shapes and energies.

Telcordia uses the curve of *Figure 3* to define the waveform's rise and decay times (Bellcore TR-EOP-000001). Test requirements also specify that both positive and negative surges be applied. While the open circuit voltage of the generator is known, the current that flows will partly depend on the characteristics of the equipment being stressed. The number of required surge variations and application repetitions varies from test to test and standard to standard.

<sup>1</sup> ITU-T (CCITT), K.11, 10/93, *Principles of Protection Against Overvoltages and Overcurrents*.

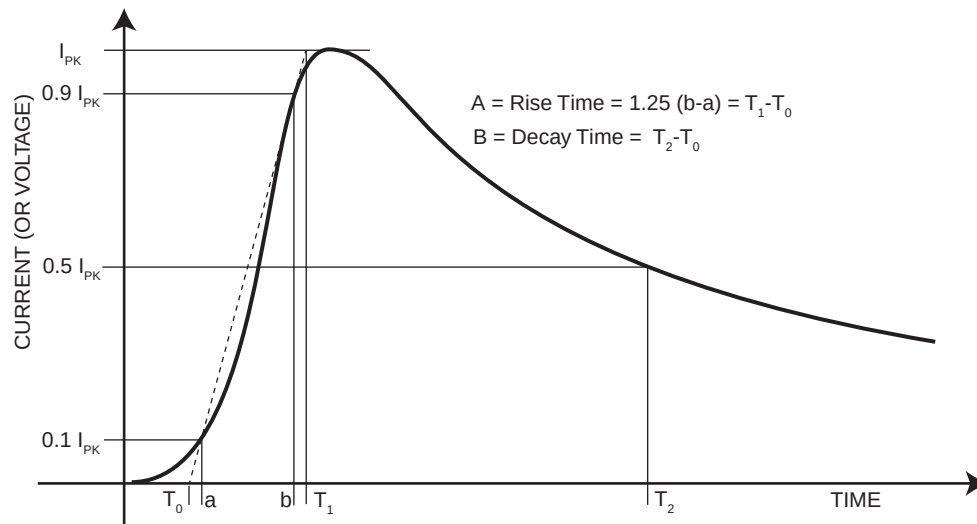
<sup>2</sup> Telcordia (Bellcore) FR-64, Issue 99, January 1999, *LATA Switching Systems Generic Requirements*.

<sup>3</sup> Telcordia (Bellcore) FR-2063, Issue 000, March 2000, *Network Equipment-Building System (NEBS) Family of Requirements (NEBSFR)*.

<sup>4</sup> Code of Federal Regulations, Title 47 – Telecommunication, Chapter I – Federal Communications Commission, Part 68 – Connection of Terminal Equipment to the Telephone Network, (revised annually).

<sup>5</sup> The National Electrical Code is sponsored and published by the National Fire Protection Association (NFPA). It is a widely accepted body of electrical equipment and installation safety standards which is typically incorporated into the building code statutes of local governmental agencies including all 50 state governments. It is revised every three years.

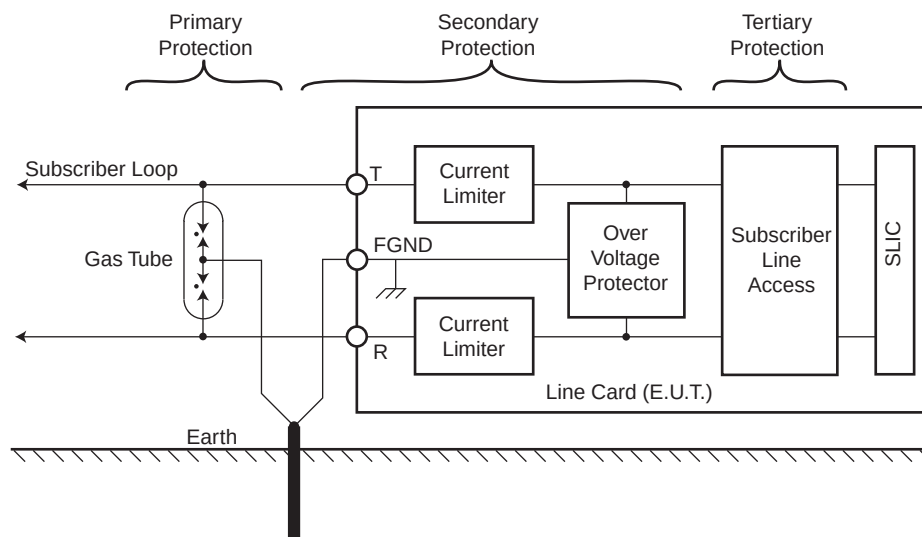
<sup>6</sup> International Electrotechnical Commission, IEC 60950 (1999-04), *Safety of Information Technology Equipment*.



**Figure 3 Double Exponential Lightning Waveform**

Besides specifying the surge waveforms differently both in shape and energy content, there are some differences in methodology between the principal standards. For the most part, GR-1089 assumes the precondition of primary protection – this would typically consist of external gas arrester tubes or carbon spark gap blocks – and so defines the test waveforms to simulate the surge energy which would “leak” past the primary protectors prior to their operation. The primary protectors are not installed for these tests. Refer to *Figure 4* below for clarification of the tiers of protection. There is some accommodation in GR-1089 for use of specific primary protection devices, e.g. gas tubes which operate at reduced voltages, provided the product specifications clearly call out the requirement for the installation of special protection. However, equipment vendors generally prefer not to have to include such a caveat in their product literature.

The ITU-T, on the other hand, often favors testing with the actual primary protectors installed between the surge generator and the E.U.T.. One clear advantage of the ITU-T method is that the effective coordination between the external primary protectors and any secondary protection incorporated into the E.U.T. is tested. The disadvantage is that the primary protectors to be used with the E.U.T. must be known. This can present a difficulty for equipment intended to be retroactively installed into a variety of existing systems where the type and condition of primary protection is uncertain. There are circumstances in which the ITU test administrator can modify the K.20



**Figure 4 Levels of Protection**

and K.21 lightning waveforms to simulate the presence of primary protectors much as in the GR-1089 approach. One should contact a recognized test facility for particulars.

**AC power fault** tests consist of connecting a power line frequency voltage generator to the E.U.T. for a specified duration, ranging from one second to many minutes, via a resistance that may be inferred from the short circuit current specification. As is the case for lightning testing, several of the ITU-T K-series power fault tests are performed with external primary protection in place to verify coordination between levels of protection.

**Test pass criteria.** Both the GR-1089 and the ITU-T tests, whether lightning surge or AC power fault, include two degrees of test severity with their respective pass criteria. The terminology associated with these are compared in *Table 1*.

Table 1 Test Severity Terminology and Pass Criteria

| Test Severity                         | GR-1089-CORE                                                                                              | ITU-T K.20, K.21                                                                                                                       |
|---------------------------------------|-----------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------|
| Term for Non-Destructive Test         | "First Level"                                                                                             | "A"                                                                                                                                    |
| Pass Criteria                         | The E.U.T. will not be damaged and it will operate as intended after the stress is removed <sup>1</sup> . | The equipment will withstand the test without damage or disturbance <sup>2</sup> and will operate properly following the test.         |
| Term for Potentially Destructive Test | "Second Level"                                                                                            | "B"                                                                                                                                    |
| Pass Criteria                         | The E.U.T. may be damaged but it may not become a fire, fragmentation or safety hazard.                   | A fire hazard does not occur in the E.U.T. and any permanent damage is confined to a small number of external line interface circuits. |

## TEST CONNECTIONS

For all test types, details of grounding and test connections are given in the test requirements as are the presence or absence of external (to the E.U.T.) protection devices, i.e. "primary protection." Most tests are repeated with differing test connections. Additionally, the E.U.T. is exposed to all test surges in all of its normal operating states. Given that many tests contain stress variations and numerous repetitions and considering the large number of combinations of test, connection and operating state, the sum total of individual tests can be a staggering figure. A regulatory compliance oriented, overvoltage protector data book<sup>3</sup> by Teccor Electronics, Inc., is an excellent quick reference guide for all the standards mentioned above.

Conceptually, both lightning surge and AC power fault generators consist of an ideal voltage source which produces the specified waveform and which is connected to the E.U.T. signal ports through known, fixed resistances. The open circuit and short circuit outputs are known. Each port or line being stressed is connected via an independent network. The manner in which the equipment is to be connected during testing is carefully specified in the test standards. In the past, multiple ports would be tested in parallel by shorting them all together and applying a single generator connection. Those days are gone; multiple output generators are available commercially and test administrators take great pains to insure testing conforms closely to the model.

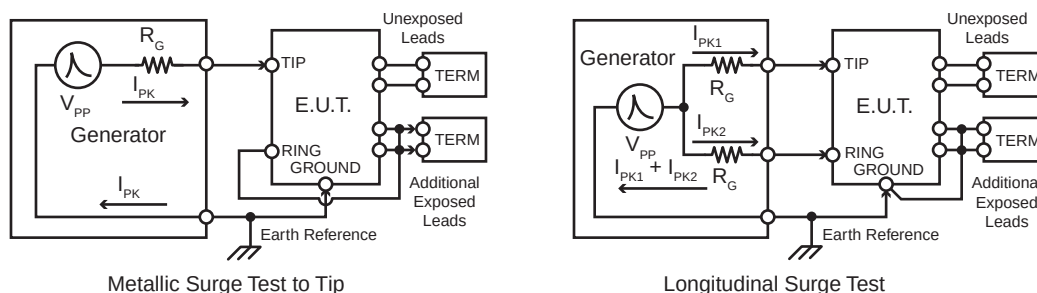


Figure 5 Basic Test Connection Methods

<sup>1</sup> In either the North American or European low severity testing, correct operation must resume without the need for manual intervention.

<sup>2</sup> A disturbance might be an occurrence such as the corruption of software or incorrect operation of fault protection facilities.

<sup>3</sup> Teccor Electronics, Inc., 1998, *SIDACTor Data Book*, Chapter 3.



With reference to *Figure 5*, two fundamentally different types of test connections are made. A differential mode surge test signal, referred to as a *metallic* signal in the Bellcore literature, is applied to all individual signal leads one at a time. These surges create large potential differences between the signal leads of the E.U.T. since all other exposed leads<sup>1</sup> are connected to the surge return line and earth ground. A common mode surge, or *longitudinal* surge, is applied to all the exposed signal leads at one time. These surges create large potential differences between the signal lines of the E.U.T. and the equipment's ground connection or between the exposed signal lines and the unexposed, ground referenced signal lines. For a 2-wire interface, this would mean Tip and Ring simultaneously. For a 4-wire interface, T, R, T1 and R1 would all be stressed at the same time. This would require a generator having four independent feeds. In some cases, up to 12 pair may be stressed simultaneously. In multiple pair interfaces, mixed mode surges are applied where longitudinal surges are applied to individual pairs while the other pairs are grounded. Practically speaking, nearly every possible connection arrangement is tested. For equipment powered from the AC power mains, the AC line connections are also tested. There is no place to hide.

### 3 DESIGN OF PROTECTION

For the most part, the line card designer will be concerned with how to implement the Secondary and Tertiary levels of protection per *Figure 4*. Understanding the circuit stress implications of the surge and power fault tests is very useful when designing the protection section of the product application.

#### 3.1 Protection Strategies

Layered protection. It is necessary that surge energy dissipation occurs in a series of stages. It is assumed in test requirements that the carbon block or gas tube primary protectors will not operate until they experience a high voltage across their terminals. Whereas a typical primary protection device may be designed to operate in the area of perhaps 300 V, GR-1089 assumes an operating point as high as 1000 V due to service wear and aging. It is also assumed that the primary protectors have enough delay in their operation to allow fast rise time surges to reach 2,500 V. And until firing voltages are reached, no surge current is shunted away from the secondary protection level. Almost needless to say, then, the amount of surge or fault energy that can be passed through this first wall of defense to the line card is vastly in excess of that required to destroy the semiconductor components of the line access and subscriber interface circuits. Depending on the durability of the SLIC and the degree of tertiary protection afforded by the LCAS, the secondary protectors to be specified may have to reduce the surge energy by several orders of magnitude.

Consider the following example. The Ring connection of a hypothetical solid state SLIC device might be able to survive a maximum power input of 300 mA at 90 V for a period of 250 ns. This works out to an energy input of about 6.8 mJ. The 10 x 1000  $\mu$ s, First Level lightning waveform specified in GR-1089 discharging into a 90 V voltage clamp element would produce a peak power input of 8.2 kW (!) and dump about 11.8 J of energy into the secondary protection. The ratio of dissipated energies in this case would be 1,750,000 to 1. Here the utility of an intervening, tertiary layer of protection at the Line Access interface can be seen. Finally, in case the impression has been given that the external primary protectors do not provide much benefit, consider also that the Bellcore requirements<sup>2</sup> for gas tube protector units (GTPUs) include being able to withstand 25 repetitions of a 10 x 250 ms,  $2,000 A_{pk}$  surge.

Basic secondary protection architecture. Again referring to *Figure 4*, a protection scheme which will pass muster must have some current limiting means in series with the line connections and some voltage limiting means in shunt either across the Tip/Ring pair, to ground or to both.

At a minimum, the current limiters must safely interrupt current flow into either of the line connections below the level which would melt the wiring. GR-1089 specifies a standard fuse to simulate the Tip and Ring wiring pair for that test. Next it must safely interrupt very high levels of lightning surge current or AC current before the line card circuits combust, fragment or otherwise create a safety hazard. Additionally, during a low severity test, the current limiter must either not open or it must reset itself shortly after the test stress is removed. Optionally, it may provide some protection for other protection elements such as the overvoltage limiting devices. Current limiting may be distributed among more than one series element but the safety interrupting portion of a distributed arrangement ought to be placed immediately closest to the card's line connections.

<sup>1</sup> Leads not associated with the set of exposed leads are terminated as in normal service. Leads which are associated with the exposed leads being tested are connected to the generator ground return with the test repeated with those same leads connected as in normal service.

<sup>2</sup> Bellcore TR-NWT-001361, Issue 1, December 1992, *Generic Requirements for Gas Tube Protector Units*, Section 4.10, Service Life Requirement.

The voltage limiters must operate with sufficient speed to prevent fast transient voltages from exceeding the absolute maximum ratings of the subscriber interface components. In this context, “fast” means  $dv(t)/dt$  values at the generator terminals on the order of 1,000,000,000 V/s. They must also be able to conduct the full fault current. As noted above, the magnitude of this current is determined by the sum of the fault generator output resistance and the line card's input series resistance. Overvoltage protection devices may be either a limiting type, such as a zener diode which attempts to clamp the voltage to a fixed maximum value, or a crowbar type such as an SCR which is switched to a very low impedance when an overvoltage condition is detected. A crowbar device is at a great advantage over a clamping device in applications where the protection operating voltage must be high, because it will experience far lower V·I power dissipation during a fault. For example, a line connection which must support unbalanced ringing may have to put the negative overvoltage protection threshold beyond -190 V to avoid false tripping.

The influence of application constraints. Application demands have a strong impact on the protection implementation. Twisted pair which must support large transverse (metallic) voltages like battery or ringing signals during normal operation require that the overvoltage limiting elements be able to discriminate between normal and abnormal conditions. Often the difference between normal and destructive voltage levels is not great requiring precision on top of robustness. This is a key issue when protecting solid state subscriber interface circuits.

Other restrictions are not hard to find. The high per card channel density of contemporary products can place very challenging circuit board real estate bounds on the protection design. This can make the use of some of the traditionally specified, durable but bulky components problematic. Performance requirements can also influence the design approach. Leakage current limits can reduce the choices of shunt elements, particularly in applications where the difference between normal and damaging voltage levels is small. Longitudinal balance requirements can reduce the options for series elements by imposing Tip and Ring resistance mismatch tolerance maximums. Incidentally, an excellent analysis of the longitudinal balance issue is presented in a SLIC related application note from Advanced Micro Devices<sup>1</sup>. In long haul applications, insertion loss limits may constrain the amount of additional series line resistance the protection circuit contributes.

Fault energy blocking versus steering. There are different approaches to reducing the power dissipation in the protection circuit elements. This arises from the fact that the amount of surge energy absorbed by the line card's protection circuit is a function of the relative impedances of the surge generator and the protection network. As one might expect from power transfer theory, the resistive elements of the protection circuit will absorb a maximum amount of surge energy when they are equal in value to the surge source output impedance. For that reason, it is helpful to know the approximate output resistance of the generator for a given test.

Lightning surge generators tend to have low output resistance, typically 10  $\Omega$  or less, while the lower stress level AC power fault generators have a higher resistance, usually over 100  $\Omega$ . If not explicitly given, the effective output resistance can be deduced from the open circuit voltage and short circuit current of the test definition. Table 2 provides some examples from GR-1089. Since having to dissipate large amounts of surge or fault energy is generally an undesirable situation for a line card, at least in terms of component bulk or cost, it is beneficial to design the protection circuit so as to avoid having an input resistance close to that of the surge and fault sources. This may be accomplished by having an input resistance relatively higher or lower than the surge source output resistance, hence the opportunity for distinct approaches.

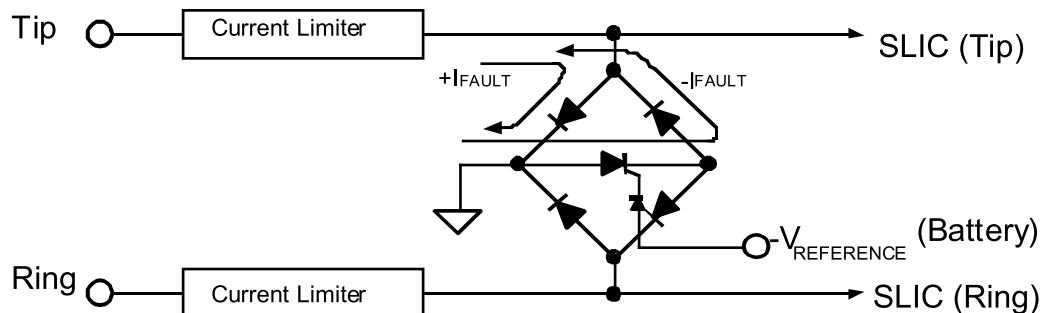
Table 2 Test Generator Output Resistance

| First Level Test Type            | Open Circuit Voltage | Short Circuit Current | Effective Generator Resistance |
|----------------------------------|----------------------|-----------------------|--------------------------------|
| 10 x 1000 $\mu$ s Lightning      | 1000 V <sub>PK</sub> | 100 A <sub>PK</sub>   | 10 $\Omega$                    |
| 2 x 10 $\mu$ s Lightning         | 2500 V <sub>PK</sub> | 500 A <sub>PK</sub>   | 5 $\Omega$                     |
| 50 V <sub>RMS</sub> , 15 minutes | 50 V <sub>RMS</sub>  | 0.33 A <sub>RMS</sub> | 152 $\Omega$                   |
| 600 V <sub>RMS</sub> , 1 second  | 600 V <sub>RMS</sub> | 1 A <sub>RMS</sub>    | 600 $\Omega$                   |

<sup>1</sup> Advanced Micro Devices, Sept. 1995, “Longitudinal Balance of AMD SubscriberLine Interface Circuits (SLICs),” AMD Publication #16230, Rev.B.

A protection circuit which has a relatively high series resistance is employing a blocking strategy to reduce the energy absorption in some of the protection components by lowering the amount of surge current flowing into the line card. Note that this approach tends to be more effective for lightning surges since that source resistance is low. High resistance circuits are less effective in AC power fault tests where the high voltage and high output resistance of the generator tend to approximate a constant current source. Many blocking type designs aim to position the series protection resistance value somewhere between lightning and AC power source resistance values, say 20 to 80  $\Omega$ . Protection resistance values higher than AC fault source values are generally too lossy to be practical in a line circuit. In some applications, the use of high breakdown voltage, high isolation parts can be employed to block current flow, e.g. a line transformer insulated adequately to withstand 2,500 V<sub>PK</sub> lightning surges.

Characteristics of a protection circuit employing an energy or current steering strategy include low input resistance and low voltage drop during operation. It seeks to reduce I<sup>2</sup>R and VI power dissipation in the protection network. A pure steering type protection design aims to maintain a small voltage drop between the point of application and the fault current return ground connection during the surge so that the bulk of the surge or fault energy is dissipated within the test generator itself rather than in the protection circuit. In order to do this, however, the protection elements must be capable of handling the maximum fault current, i.e. the generator's rated short circuit output current. One example of current steering is depicted in *Figure 6* below.



**Figure 6 Current Steering Example**

In this circuit, voltages more than 1 diode drop above ground are shunted to ground, away from the SLIC. Voltages two or three volts less than the reference voltage, -48 VDC battery for example, will cause the SCR to switch on, again shunting current to ground. This approach is particularly useful for protecting solid state SLICs, as discussed in another good application note from AMD<sup>1</sup>. Solid state SLICs generally require precise overvoltage control. Care must be taken to use parts which are fast enough and to supply sufficient operating current to any crowbar type devices to achieve the speed necessary to adequately limit voltage overshoot during the fast rise times noted above. Note, by the way, that as the circuit of *Figure 6* stands, the presence of ringing voltage would be treated as a fault condition.

Component selection and ratings tradeoffs between the series and the shunt protection components. Quite often, a solution will combine elements of both blocking and steering strategies. For example, if the SCR of *Figure 6* is rated to handle GR-1089, 10 x 1000  $\mu$ s exponential decay surges having a peak current of 60 A<sub>PK</sub> rather than the full 100 A<sub>PK</sub> short circuit output of the surge generator, series resistance must be added in the current limiting blocks to reduce the surge current flow into the line terminals to 60 A<sub>PK</sub>. Knowing the generator has an output resistance of 10  $\Omega$  (Table 2), an additional 6.7 ohms would be needed at a minimum. That value will cause efficient energy transfer into the resistor, however. A careful analysis shows 17.3 J would be dumped into this component.<sup>2</sup> If the application can tolerate 50  $\Omega$  in each lead, then the resistors would only have to be able to absorb 10.1 J and the SCR rating requirement would drop to 16.7 A<sub>PK</sub>. Meanwhile, in the case of the AC power fault test with 600 VRMS exposure for 1 second, the short term I<sup>2</sup>R power stress<sup>3</sup> for the resistor would have increased from about 6.6  $\Omega$  to 42.6  $\Omega$ . The rating tradeoff in this example may or may not be good depending on the characteristics of preferred components.

The components employed in line circuit protection must either be rated in a useful manner by the component manufacturer or must be tested in the application. Most standard electronic components are not adequately

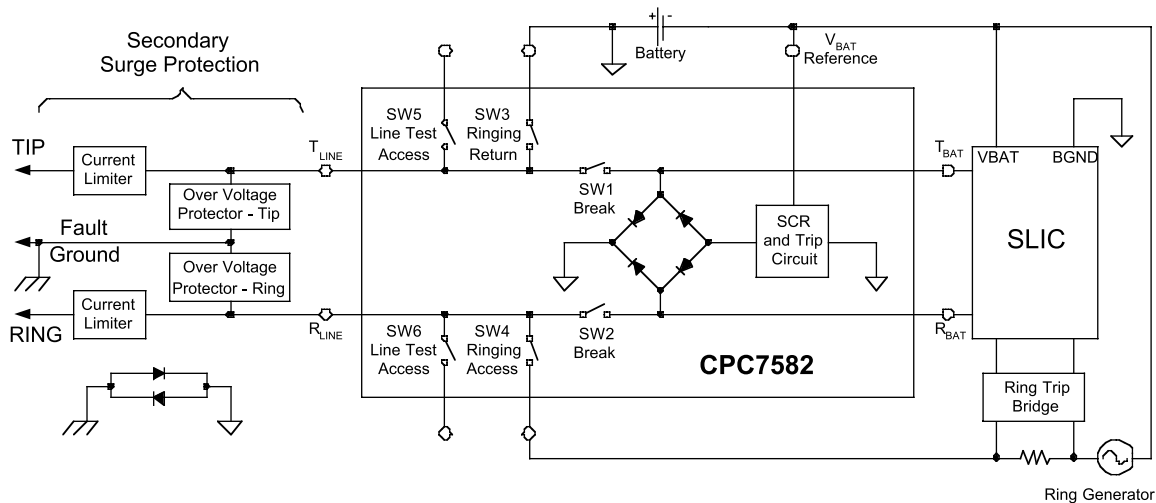
<sup>1</sup> Advanced Micro Devices, July 14, 1999, "Generic SLIC Device Surge Protection," AMD Publication #22648, Rev.A.

<sup>2</sup> See Appendix Item 4.1, *The Energy Transferred by a Lightning Surge*.

<sup>3</sup> See Appendix Item 4.2, *Power Dissipation During an AC Power Fault*.

characterized for pulse applications let alone the specialized pulse waveforms used during compliance testing. In the experience of the author, it is rarely intuitive how well a particular device will hold up to a lightning surge. Current crowding effects can generate hot spot blowouts in surprisingly stout looking power resistors for example. Fortunately, there are a number of electronic products which target the telecommunications market. These can be real time savers. A few sources are provided in the Appendix, Item 4.3.

Additional protection elements provided by the solid state access switch. The LCAS (Line Card Access Switch) is equipped with a current limiting and steering protection circuit along the lines of *Figure 6* above. The design of the secondary protection is thereby significantly simplified. At  $\pm 320\text{ V}^1$  the breakdown voltages of the access switches are much greater than those of the SLIC's tip and ring connections which typically run a few volts to either side of the battery voltage. Even so called high voltage SLICs do not yet approach such high withstand potentials. Note that the circuit of *Figure 6* conveniently clamps within a volt or two of the battery supply. This provides the necessary protection for the SLIC while simultaneously affording flexibility in the ringing scheme, e.g. balanced or unbalanced, and bringing the ringing supply equipment under the umbrella of the secondary protection. *Figure 7* below provides an overview of how the secondary surge protection circuit of the line card and the tertiary protection integrated into the LCAS may be coordinated in the SLIC protection system.



**Figure 7 Tertiary Protection Components Provided by the LCAS**

The Secondary Protection blocks or deflects the bulk of the surge energy away from the  $T_{\text{LINE}} / R_{\text{LINE}}$  pins of the LCAS. In the process, the peak voltage appearing at those pins remains below the rated breakdown level. The LCAS is then in a position to further limit the peak voltage appearing at the  $T_{\text{BAT}} / R_{\text{BAT}}$  connections to the SLIC (break switches SW1 and SW2 closed) within safe limits. There is a key protection feature of the LCAS not shown in this figure. Break switches SW1 and SW2 each incorporate an additional current limiting function which does not permit steady state current flows in excess of  $\pm 250\text{ mA}$ . This is necessary to allow sufficient voltage to be developed on the  $T_{\text{LINE}}$  and/or  $R_{\text{LINE}}$  pins during a surge to operate the far more robust overvoltage protectors in the secondary. Otherwise, the break switches, the diode bridge and the SCR circuit of the LCAS integrated circuit would be forced to conduct the entire fault current until they failed, clearly an impractical situation. This is covered in more detail in the next section.

### 3.2 Design Examples for Protected Solid State Line Interface

Subscriber interface. *Figure 8* below details a circuit which interfaces a 4-wire analog voice frequency connection from a CODEC to a 2-wire subscriber loop. Although the circuit is analog, it is able to be completely controlled by logic level signals from a microcontroller. The primary components are an Advanced Micro Devices Am7946 SLIC<sup>2</sup> which handles battery feed, line detection and signaling functions and an IXYS ICD CPC7582 Line Card Access Switch which handles ringer switching, test bus access to the subscriber loop and SLIC protection. The LCAS automatically isolates the line in case of loss of battery voltage. Note that additional LCAS configurations are available which contain either fewer or more line and ringing testing provisions.

<sup>1</sup> Appropriately, the integrated ringer switches in the LCAS have breakdown voltage thresholds considerably higher.

<sup>2</sup> Advanced Micro Devices, January 1998, "Am7946 Subscriber Line Interface Circuit," AMD Publication #19754, Rev:B.

Table 3 Current Consumption versus Operating State

| State                  | Battery Current ( $-48 V_{DC}$ ) | Low Voltage Current ( $+5 V_{DC}$ ) |
|------------------------|----------------------------------|-------------------------------------|
| Off                    | -0.4 mA                          | 3.1 mA                              |
| Standby (On-Hook)      | -0.6 mA                          | 4.3 mA                              |
| Active-Idle (On-hook)  | -4.9 mA                          | 8.0 mA                              |
| Active-Talk (Off-Hook) | -28.7 mA                         | 8.9 mA                              |

The design specifications provide for a nominal battery voltage of  $-48 V_{DC} \pm 8 V_{DC}$ , a  $900 \Omega$  loop impedance and a 25 mA loop current. The user defined 4-wire to 2-wire gain is set to  $-3$  dB. The 2-wire to 4-wire and 4-wire to 4-wire gains are both fixed at  $-6$  dB. The ring trip detection circuit is configured for unbalanced ringing biased to the negative battery source. Typical current consumption values are given in the following table.

The absolute maximum ratings relevant to surge and fault testing for the **Am7946 SLIC** are as follows.

- VBAT with respect to AGND/DGND [Recommended operation  $-40$  V to  $-58$  V.]
- Continuous  $+0.4$  V to  $-80$  V
- 10 ms  $+0.4$  V to  $-85$  V
- BGND with respect to AGND/DGND  $+3$  V to  $-3$  V [Recommended operation  $\pm 100$  mV.]
- A(TIP) or B(RING) to BGND
- Continuous  $-70$  V to  $+1$  V
- 10 ms ( $f = 0.1$  Hz)  $-70$  V to  $+5$  V
- 1ms ( $f = 0.1$  Hz)  $-80$  V to  $+8$  V
- 250 ns ( $f = 0.1$  Hz)  $-90$  V to  $+12$  V

Some key absolute maximum ratings for IXYS ICD's **LCAS family** are

- VBAT with respect to DGND  $-85$  V [Recommended operation  $-19$  V to  $-72$  V.]
- Pole-to-pole switch isolation  $\pm 330$  V [Recommended operation  $\pm 320 V_{MAX}$  @  $25^\circ\text{C}$ .]
- Power ringer switch isolation  $\pm 465$  V @  $25^\circ\text{C}$
- Protection SCR hold current<sup>1</sup> 70-110 mA

**Grounds.** The circuit uses three distinct grounds. These are Battery Ground (BGND) which is the return for the  $-48$  VDC battery supply, Analog and Digital Ground (AGND/DGND) which is the combined signal ground for the circuit, and Fault Ground (FGND) which is the *intended* return path for fault currents. In order to avoid component damage during system power-up or maintenance, AGND/DGND and FGND are held within  $\pm 1$  V of BGND by anti-parallel diodes. During normal operation, when potential differences between grounds are small, the diodes provide good signal isolation between grounds. Diodes between FGND and BGND may be disadvantageous, however, if there is substantial ground bounce at the FGND connection during fast rise time surges. Please refer to section 3.3 below for a discussion of ground bounce.

**Specifying Over Voltage Protection thresholds – a first cut.** The protection thresholds must be set low enough so that the circuit is protected but high enough to permit normal operation and avoid nuisance tripping. The values to be determined are  $V_S$ , the guaranteed protection operating voltage, and  $V_{DRM}$ , the minimum required working or non-operating voltage. There are three basic cases to be considered.

<sup>1</sup> Will vary depending upon which version of LCAS selected.





- $$|V_{BAT}|_{MAX} + |V_S| < |V_{BR\_SW1}|_{MIN}$$

- **Case 2.** The breakover voltage of the LCAS power ringing switches SW3 and SW4 must not be exceeded while in the off state. Consequently, the worst case peak ringing voltage plus the guaranteed protection switching voltage must not exceed the minimum isolation voltage of the ring switch. For the CPC7582, the minimum ring switch (SW4) isolation rating is increased to  $\pm 455 \text{ V @ } -40^\circ\text{C}$  to accommodate unbalanced, battery backed ringing.

$$|V_{BAT}|_{MAX} + |V_{RING\_PK}|_{MAX} + |V_S| < |V_{BR\_SW4}|_{MIN}$$

If worst case ringer voltage is limited to  $86 V_{RMS}^1$ , then

$$|-56| + |\sqrt{2} \cdot 86| + |V_S| < |455| \quad \text{or} \quad |V_S| < 277 \quad V_{PK}.$$

In this design, it is seen that the limitation of the LCAS break switches is of greater concern than that of the ring switch. The ring return switch, SW3, lacks the enhanced isolation rating of SW4 having the same  $\pm 310 V @ -40^\circ C$  rating as the break switches. On the other hand, in this application example, it is never exposed to ringing voltage peaks and the analysis of Case 1 would suffice.

- **Case 3.** During ringing, the overvoltage protectors in the secondary must not operate. This guaranteed “working voltage” is called  $V_{DRM}$ . Therefore,

$$|V_{BAT}|_{MAX} + |V_{RING\_PK}|_{MAX} - |V_{DRM}| < 0$$

Again set an  $86 V_{RMS}$  maximum limit on the ringing generator output. First consider the most negative excursion. From our requirements, the most negative battery voltage is  $-56 V_{DC}$  so that

$$-56 - \sqrt{2} \cdot 86 - V_{DRM}^- > 0 \quad \text{or} \quad V_{DRM}^- < -178 \quad V_{PK}.$$

For the case of the most positive excursion, the least negative battery voltage must be used which we had set to  $-40 V_{DC}$ . Then the calculation becomes

$$-40 + \sqrt{2} \cdot 86 - V_{DRM}^+ < 0 \quad \text{or} \quad V_{DRM}^+ > +82 \quad V_{PK}.$$

This suggests the possibility of using asymmetric positive and negative working voltages for the Ring lead overvoltage protector. Additionally, the Tip lead does not need to support ringing voltage in the present case. It does need to support battery voltages, since battery reversal signaling could be used. Manufacturers of over-voltage protection devices targeted at this application have, in fact, settled upon different switching and working voltages for Tip and Ring.

So far, it has been established that the breakover voltages of the OVP devices should fall within the ranges of

$$\begin{aligned} -254 &< V_{S\_RING}^- \leq V_{BR\_RING}^- \leq V_{DRM\_RING}^- < -178 \quad V_{PK}, \\ +82 &< V_{DRM\_RING}^+ \leq V_{LIM\_RING}^+ \leq V_{S\_RING}^+ < +254 \quad V_{PK} \quad \text{for Ring and} \\ -254 &< V_{S\_TIP}^- \leq V_{LIM\_TIP}^- \leq V_{DRM\_TIP}^- < -56 \quad V_{PK}, \\ +? &< V_{DRM\_TIP}^+ \leq V_{LIM\_TIP}^+ \leq V_{S\_TIP}^+ < +310 \quad V_{PK} \quad \text{for Tip.} \end{aligned}$$

There does not seem to be a compelling reason to distinguish between positive and negative voltages on the Tip lead. We should apply the most restrictive range to both polarities using symmetry in order to simplify the protection design. There could be some benefit to asymmetric thresholds on the Ring lead if the goal is to reduce voltage stress on the LCAS to the extent practical whether or not it is needed<sup>2</sup>. Too, that choice may hinge on other system considerations. For example, we have not considered the range of voltages which may appear on the Test Access switches, SW5 and SW6 with the implications of having multiple line cards sharing a common test bus.

<sup>1</sup> For non-sinusoidal ringing waveforms, use the actual peak voltage rather than  $\sqrt{2} \cdot V_{RING\_RMS}$  or apply the correct crest factor.

<sup>2</sup> Standalone GR-1089 testing of the reference circuit did not demonstrate the need for asymmetric Ring protection.

There are other factors which will have a bearing on these limits, but the most significant is probably the longitudinal voltages appearing at the Tip and Ring leads due to power line induction while the line circuit is presenting a high longitudinal impedance to the line. These voltages must not cause operation of the overvoltage protectors since the equipment must operate properly when exposed to such induced voltages per GR-1089, etc. The estimation of  $|V_{DRM}|$  for the operating modes other than ringing is beyond the scope of this note. Pending actual product testing, however, one can accept some guidance from the overvoltage protection device manufacturers who have successfully targeted integrated access switch applications. Two such examples will be presented below.

**Selecting secondary protection architecture.** There have been many different protection schemes proposed and applied over the years as various technologies have developed. Some of the older technologies are less suited for protection of solid state interface devices because they lack sufficient precision and dynamic range. For instance, metal oxide varistors would fall into that category due to their relatively soft clamping characteristic. Others possess at least one highly attractive feature which, nevertheless, is not especially advantageous in this situation or which does not overcome its shortcomings. *Table 4* lists a few common protection devices which were not deemed appropriate in the example circuit solutions together with a brief description of the problematic parameters in the context of this application. Sources for a variety of line circuit protection components are given in Appendix 4.3.

Table 4 Less Appropriate Protection Component Types

| Protection Component               | Circuit Function     | Problematic Parameters                                                       |
|------------------------------------|----------------------|------------------------------------------------------------------------------|
| Metal Oxide Varistor               | Over Voltage Limiter | Operating voltage tolerance, maximum clamping voltage, wear.                 |
| Zener Diode or TVS <sup>1</sup>    | Over Voltage Limiter | Power dissipation, maximum clamping voltage, junction capacitance.           |
| Gas Discharge Tube                 | Over Voltage Limiter | Operating voltage range and tolerance, speed.                                |
| Power Resistor                     | Current Limiter      | Circuit board real estate, surge withstand capability.                       |
| PTC <sup>2</sup> Thermistor Switch | Current Limiter      | Resistance tolerance and stability, fault interrupt capacity, tempco, speed. |

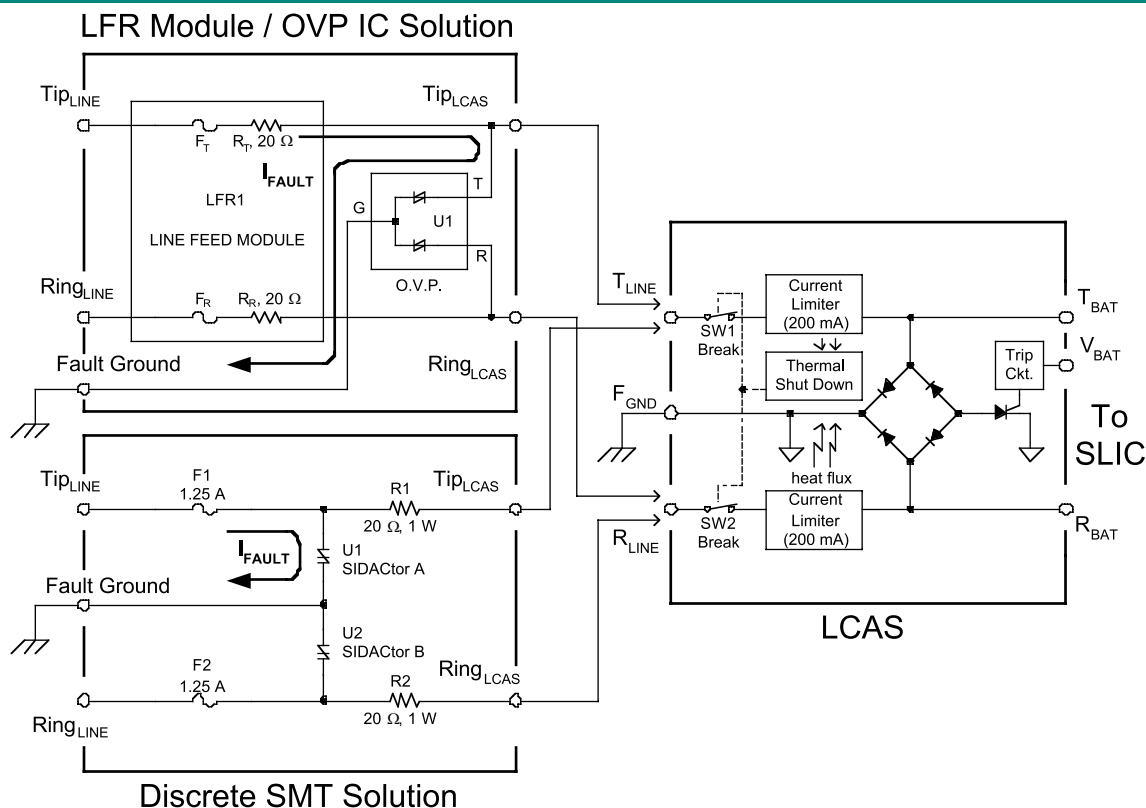
*Figure 9* illustrates two examples of proven circuits and also shows the protection components internal to the LCAS so that the coordination between the secondary and tertiary elements may be visualized. The approach taken here relies on crowbar type overvoltage protection and highly compact current limiting components. In both circuits, the selected OVP components are able to abruptly clamp very fast rise time surges and, when the surge current rises to their respective switching current thresholds (under 1 A), to switch to a very low impedance state in which they dissipate less power. There is small danger of overheating because as these parts warm up in a zener-like clamping mode, the switching current threshold drops until switching occurs. If the current buildup is fast, the clamping phase is extremely brief; the devices crowbar immediately. As remarked earlier, it is the current limiting ability of line break switches SW1 and SW2 in the LCAS that forces the surge or fault current to flow through the OVPs in the first place. In cases where the fault voltage is too low to fire the OVPs, the resulting temperature rise in the LCAS current limiter forces the break switches to open via a Thermal Shut Down mechanism. This feature eliminates failures due to so called “sneak under” faults and obviates the need for self-resetting current interrupters in the Tip and Ring circuits. Incidentally, this condition may be sensed at the TSD pin of the CPC7582 so that appropriate alarm actions may be taken.

The key differences between the two circuits revolve around current limiting. Both ultimately rely on fuses to limit destructive (Second Level or B Level) currents which could otherwise result in burning wire and other safety hazards. Each also includes 20  $\Omega$  of series resistance in the Tip and Ring leads although they do not serve identical functions. The LFR Module solution uses thick film hybrid technology to integrate the fuse function for both Tip and Ring with the respective fixed resistors. These resistors are included in the fault current path. The Discrete SMT solution uses individual, albeit very compact, surface mount Tip and Ring fuses with no fixed resistors in the fault current path. The first solution tends somewhat toward the current blocking strategy discussed earlier while the second leans more toward the current steering strategy. Fault currents are similar in the two circuits for AC power fault conditions but the LFR Module solution experiences distinctly lower peak currents during lightning surges. This permits the use of a more compact OVP device at the expense of the greater overall bulk of the LFR module itself. In the Discrete SMT component solution, high peak currents are allowed to flow during

<sup>1</sup> Transient Voltage Suppressor. A zener diode device characterized for surge duty. Please refer to Appendix 4.2 for an analysis of power dissipation in zener diodes during AC power faults.

<sup>2</sup> Positive Temperature Coefficient.





**Figure 9 Example Secondary Protection Circuit Solutions**

lightning surges. The OVPs are specifically rated to handle these large currents. This approach permits a very compact construction but requires a very low fault ground path impedance to avoid ground bounce problems.

For both solutions, the 20  $\Omega$  resistors serve to limit conducted EMI from the line card into the system and to enhance the phase margin of the SLIC's line driving amplifiers by providing some isolation from the line capacity should it be required in any particular case. SLIC application literature typically suggests series resistance values from 20  $\Omega$  to 50  $\Omega$  in each lead. The lower value was used in this case in order to permit an additional 60 ohms of loop length while still limiting peak surge currents to the maximum rating of the OVP device selected for the LFR Module solution. LFR modules are available with various resistance values to suit the particular application.

Table 5 below contains the bill of materials for each of the secondary protection solutions. Both circuits are known to pass the requirements of GR-1089 for central office equipment. The equipment designer will need to look at a variety of manufacturing and application specific factors in order to determine the most suitable approach.

Table 5 Secondary Protection Parts Lists

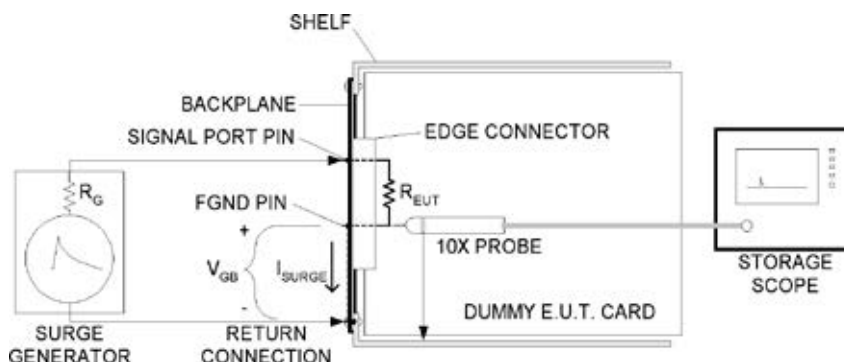
| Solution       | Designators | Manufacturer | Part Number   | Description                                                                                                      |
|----------------|-------------|--------------|---------------|------------------------------------------------------------------------------------------------------------------|
| LFR Module     | LFR1        | MMC          | L11A020AA     | TF <sup>1</sup> Resistor/Fuse Module, 20 $\Omega$ , through hole, 1.89" L x 0.42" H x 0.13" T, GR-1089 qualified |
| Discrete Fuses | F1, F2      | Littelfuse   | FI 250T       | SMT Fuse, 1.25A, 250V, 18.2A <sup>2</sup> s, GR-1089 rated <sup>2</sup>                                          |
| "              | R1, R2      | KOA Speer    | RK73H3A_20R0F | SMT Resistor, 20 $\Omega$ , 1%, 1W, 2512 case size                                                               |
| "              | U1          | Littelfuse   | P1200SCL      | SMT SIDACtor, $\pm 130V_{MAX}$ 500 A (2x10ms), DO-214AA                                                          |
| "              | U2          | Littelfuse   | P2000SCL      | SMT SIDACtor, $\pm 220V_{MAX}$ 500 A (2x10ms), DO-214AA                                                          |

<sup>1</sup> TF = Thick Film, SOIC-8 = Small Outline IC, 8-pin (JEDEC type PDSO-G8), SMT = Surface Mount Technology component.

<sup>2</sup> Meets required repetitions of 500 A (2x10ms), 100 A (10x1000ms), 1 A<sub>RMS</sub> (1 s) without external, current limiting resistor. Interrupts 600 V<sub>RMS</sub> @ 60 A<sub>RMS</sub>.

## 3.3 Other Considerations

**Fault Ground bounce.** The FGND connections to the secondary and tertiary protection circuits should insure that nearly all fault current flows in the system protection ground rather than in the power supply returns. This is beneficial in that system disturbances will be minimized but it could be stressful for the LCAS. Note that during surge conditions, any increase in the potential of FGND relative to BGND due to surge current flow will directly add to the surge voltage stress applied to the LCAS switches. This is because those switches generally have some, if not most poles connected to signals which are referenced to BGND. The effectiveness of the fault ground connection ought to be verified, particularly if the fault current path resistance is very low. Please refer to *Figure 10*.



**Figure 10 Ground Bounce Measurement**

Consider the GR-1089 First-Level Lightning test which applies a longitudinal  $2 \times 10 \mu\text{s}$  surge having a short circuit current capacity of  $500 A_{PK}$  per conductor. In a 2-wire interface, the FGND terminal could carry up to  $1000 A_{PK}$  achieving this value at a rate of  $5 \times 10^8 \text{ A/s}$ . It would take very little inductance in the FGND path to produce a significant voltage drop. Since a ground bounce signal could be developed at the rate of  $0.5 \text{ V} / \text{nH}$  of FGND path inductance.

$$v(t) = L \frac{di(t)}{dt}$$

An additional ohmic contribution of  $0.5 \text{ V} / \text{m}\Omega$  of contact resistance is possible at the current peak. The generator return connection instructions contained in GR-1089<sup>1</sup> are actually designed to minimize ground bounce but, even so, it's clear that an extremely low Fault Ground impedance is essential in a robust design. With careful technique<sup>2</sup>, ground bounce measurements may be performed on the equipment enclosure in advance of actual product design. In *Figure 10* above, a storage oscilloscope is used to capture the voltage,  $V_{GB}$ , developed across the connector+backplane circuit path, designated  $I_{SURGE}$ , between the FGND circuit node on the dummy line card and the shelf.  $R_{EUT}$  is the proposed current limiting impedance of the secondary protection circuit. This impedance may be resistive or complex. If significant ground bounce is present, the use of bonding diodes between FGND and BGND may need to be reconsidered since disruptive fault currents may then flow through BGND. In that case, resistor, e.g.  $100$  to  $1000 \Omega$ ,  $1 \text{ W}$ , may serve instead.

**Printed circuit board and backplane layout considerations.** This is the right moment to emphasize the importance of PCB layout, particularly those circuit nodes included in the fault current paths indicated in *Figure 9*. The entire current path, from Tip or Ring to the equipment frame must be considered. This includes connector pin assignment and the routing of fault ground on the backplane in from-scratch system designs. On the line card itself, the traces ought to be as short and as wide as practical. Protection components must be placed immediately adjacent to the Tip and Ring entry. If the PCB is multi-layer, avoid allowing the BGND or AGND/DGND planes to extend into the region containing the secondary protection components. Wide isolation bands can be used to subdivide affected power planes appropriately with the segregated areas providing an excellent medium to route FGND to the edge connector – use multiple vias to stitch SMT pads to such inner layers. The

<sup>1</sup> Per section 4.5.7, *First-Level Lightning Surge Tests (Telecommunications Port)*, "The ground return connection for the surge test generator should be as close to the EUT as possible. Preferably to the equipment framework that contains the EUT."

<sup>2</sup> The test arrangement is subject to large common mode signals between the generator and the oscilloscope frame that the oscilloscope may not be able to completely reject. This can largely mask the sought after difference signal. Even worse, the 10X probe ground lead is susceptible to magnetic coupling to the surge current path. The length and placement of the ground probe will have a great affect. Check by capturing waveforms when the 10X probe is connected to the same point as the probe's ground lead; if the setup is clean, only a small signal will be seen. Using the equipment shelf to shield the probe, as suggested in the figure, may help somewhat. The generator's test leads ought to be a short twisted pair. It may be necessary to use differential probe techniques in addition to maximizing isolation between the generator, the E.U.T. and the oscilloscope.

implications for the card's connector pin assignment are clear. Tip, Ring and FGND must be immediately adjacent to one another. Connector contact impedance may bear close scrutiny and multiple pins dedicated to FGND ought to be given serious consideration. When faced with an existing connector pin assignment having an unfavorable FGND location, the designer should give extra weight to the blocking strategy used in the LFR Module approach. Finally, do not neglect to maintain sufficient clearance between traces. Arcing during fault application will defeat the correct operation of the protection design.

SCR and OVP hold currents. In order to release from their low impedance states following a surge or power fault, the direct current flowing through these crowbar devices must fall below their rated minimum hold currents,  $I_H$ . This is 70 mA for the SCR in the CPC7582 and over 100 mA (more typically  $\pm 150$  mA) for all of the OVP devices listed. Consequently, the direct current output capability at the SLIC circuit's Tip and Ring pins must not exceed  $\pm 80$  mA under short circuit conditions.

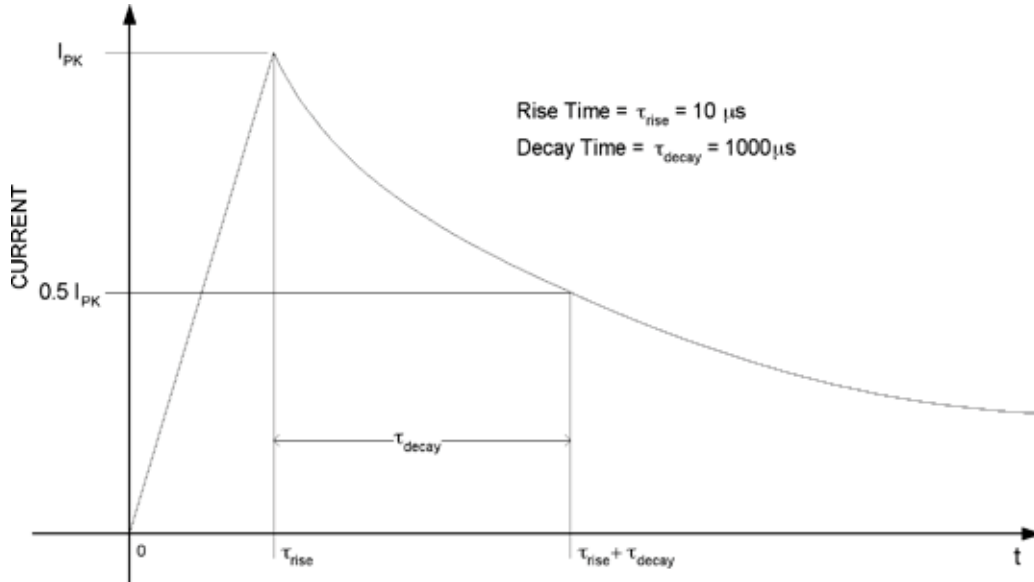
Miscellaneous considerations. A number of considerations arise from the nature of the application and system design.

- Card mix in the equipment shelf. When line cards share a common test bus, the worst case voltages appearing on the bus must be taken into account since the Test Access switches SW5 and SW6 of the CPC 7582 have the same  $\pm 320$  V @ 25°C limitation as the other switches. The scenario that comes to mind is having the test bus connected to a Tip and Ring pair while that same line is experiencing a continuous AC power fault condition. This would subject the test access ports of all the other line cards to the fault waveform as determined by the secondary protection on the fault exposed card. Line cards designed for use in proprietary equipment environments may be able to take advantage of having identical overvoltage protection limits on Tip and Ring. Where unknown card types share the test bus, worst case bus voltages may exceed the limits of SW5 and SW6. Consider especially the case where one of the LCAS equipped line cards is simultaneously supplying ringing.
- Test bus restrictions and test access switch protection. For the kinds of reasons mentioned above, it may well be necessary to restrict the maximum voltages either on the test bus itself or on a per line card basis. When the service environment is not fully understood or controlled, it would probably behoove the designer to be conservative and to add strong overvoltage protection at the test access pins of the LCAS. Such protection may or may not need not be as robust as the main secondary protection depending on the specification of the bus. In systems containing a common card with test bus overvoltage limiters, those voltage limits must be discovered and factored into the design. The specifications of the metallic loop test system (MLT) need to be understood as well in order to take advantage of the greatest amount of series resistance in the test access permitted. The worst case would be sharing an unprotected test bus with a line card which establishes a direct metallic test connection to the line side of its own secondary protectors. Then the first test access port OVP to fire could draw the full fault current.
- xDSL and xDSL + POTS applications. Designers of applications in which subscriber terminal equipment is to be powered via the loop must pay careful attention to the possibility of delivering current to OVP components in excess of their hold currents.

## 4 APPENDIX

### 4.1 The Energy Transferred by a Lightning Surge.

A good approximation of the 10 x 1000  $\mu$ s, double exponential waveform, consistent with the earlier definition of lightning surge rise time, is made by assuming a linear current rise followed by an exponential decay as sketched in the figure below (not to scale). In any case, only a small amount of the total pulse energy is contained in the rise time.



**Figure 11 Approximation of the 10 x 1000 ms, Double Exponential Waveform**

Energy is absorbed in the E.U.T. when the surge current flows through resistive elements, lumped together as  $R_{EUT}$  or through constant voltage elements. Examples of constant voltage elements are diodes in forward conduction, zener diodes in reverse avalanche and semiconductor crowbar devices in their on state. As a first order approximation, all these series fixed voltage drops may be lumped together as  $V_{CLAMP}$ , the peak voltage seen at a protected circuit node. If the open circuit peak voltage of the surge generator is  $V_{PP}$  the resistance looking into the E.U.T is  $R_{EUT}$  and the generator's output resistance is  $R_{GEN}$ , then the effective

$$V_{PK} = V_{PP} - V_{CLAMP} \quad \text{and the effective peak current is}$$

$$I_{PK} = \frac{V_{PK}}{R_{GEN} + R_{EUT}}$$

The expression for current as a function of time is given by

$$i(t) = \begin{cases} 0 \leq t < \tau_{rise} : \frac{I_{PK}}{\tau_{rise}} \cdot t \\ t \geq \tau_{rise} : I_{PK} \cdot e^{-\left(\frac{\ln 2 (t - \tau_{rise})}{\tau_{decay}}\right)} \end{cases}$$

The instantaneous power dissipated in the constant voltage elements is then  $p_V(t) = V_{CLAMP} \cdot i(t)$ . The total pulse energy absorbed by the voltage clamping elements in the discharge path can be found by integrating this power over time from  $t = 0$  to  $t = \infty$ . This may be expressed

$$E_V = V_{CLAMP} \cdot \left( \int_0^{\tau_{rise}} i(t) dt + \int_{\tau_{rise}}^{\infty} i(t) dt \right)$$

which evaluates to

$$E_V = V_{CLAMP} \cdot I_{PK} \cdot \left( \frac{\tau_{rise}}{2} + \frac{\tau_{decay}}{\ln 2} \right)$$

If there are two or more constant voltage elements in series in the discharge path, the energy absorbed by each is simply in proportion to its voltage drop relative to  $V_{CLAMP}$ . It should be mentioned that selecting an OVP device to achieve the required clamping voltage entails some analysis. (For zener diode based protectors, e.g. Transient Voltage Suppressors (TVS), it is helpful to refer to the manufacturers' applications notes<sup>1</sup> to guide the process. Applying power voltage regulator zener diodes is somewhat more problematic since behavior under pulse conditions is usually less well specified.)

The instantaneous power in the resistive elements in the discharge path is proportional to the square of the current as follows.

$$p_R(t) = R_{EUT} \cdot i(t)^2 \text{ where}$$

$$i(t)^2 = \begin{cases} 0 \leq t < \tau_{rise} : \left( \frac{I_{PK}}{\tau_{rise}} \right)^2 \cdot t^2 \\ t \geq \tau_{rise} : I_{PK}^2 \cdot e^{-\left( \frac{\ln 4(t - \tau_{rise})}{\tau_{decay}} \right)} \end{cases}$$

The total pulse energy absorbed by a resistive element can be found by integrating power over time to  $t = \infty$ .

$$E_R = R_{EUT} \cdot \left( \int_0^{\tau_{rise}} i(t)^2 dt + \int_{\tau_{rise}}^{\infty} i(t)^2 dt \right)$$

Which evaluates to

$$E_R = R_{EUT} \cdot I_{PK}^2 \cdot \left( \frac{\tau_{rise}}{3} + \frac{\tau_{decay}}{\ln 4} \right)$$

If the integration is performed numerically, integrating out to  $t = 10 \cdot \tau_{decay}$  provides more than sufficient accuracy.

The total energy transferred to the E.U.T. during the surge is the sum  $E_V + E_R$ . Table 6 shows a few examples of energy dissipation versus the protection circuit configuration. The energy transfer table doesn't tell the whole story. The peak instantaneous power can be important when selecting protection components also. The instantaneous power expressions for resistance and voltage elements can be evaluated at the current peak to determine the maximum power stress, i.e.  $p_V(\tau_{rise})$  and  $p_R(\tau_{rise})$ . These values can be astoundingly high. A prevalent mechanism for component failures in this type of stress testing is hot spot generation due to current crowding. For example, film resistors must be adequately sized to avoid excessive current densities in the conductive surface layer which can lead to dramatic blowouts.

<sup>1</sup> Bruce Hartwig, General Semiconductor, "Determining Clamping Voltage Levels for A Broad Range of Pulse Currents," QuikNote Series: No. 101. (Currently available on line at General Semiconductor, <http://www.gensemi.com/appnotespdf/quik101.pdf>.)

**A note on fuses:** For fast fault current surges, fuses are frequently specified by an ampere-squared \* time product,  $I^2 \cdot \Delta t$ , in addition to the standard, slow fault fusing current rating. If  $R_{EUT}$  is set to unity in the expression for  $E_R$ , the amp-squared second product will be calculated and can then be compared to the candidate fuse rating. Be aware, however, that meeting the  $A^2$  second specification is not all that is required for safe operation. A manufacturer marketing a fuse for surge applications should also provide the maximum safe interrupting current rating at a usefully high test voltage, e.g. 600 V<sub>RMS</sub>, for AC power fault conditions. Bare, tubular glass case fuses can shatter during Second Level or B Level AC power fault testing due to the extremely abrupt increase in internal gas temperature and pressure.

Table 6 Lightning Surge Energy Examples – 10 x 1000  $\mu$ s, 1000 V, 100 A

| E.U.T. Resistance         | E.U.T. Clamp Voltage | $E_R$   | $E_v$   | $E_{Total}$ |
|---------------------------|----------------------|---------|---------|-------------|
| 10 $\Omega$ ( $R_{GEN}$ ) | 0 V                  | 18.08 J | 0.00 J  | 18.08 J     |
| 0 $\Omega$                | 100 V                | 0.00 J  | 13.03 J | 13.03 J     |
| 50 $\Omega$               | 100 V                | 8.15 J  | 2.17 J  | 10.32 J     |
| 0 $\Omega$                | 5 V                  | 0.00 J  | 0.72 J  | 0.72 J      |

## 4.2 Power Dissipation During an AC Power Fault

AC power fault tests are of long duration relative to the thermal time constants of the protection components. Some tests in GR-1089 run for 15 minutes. Component temperatures reach steady state levels in that amount of time and the required power ratings and temperature rise calculations should be based on continuous duty for those tests. Even the short duration tests, on the order of one second, are long enough and stressful enough to achieve very significant general heating.

**Power dissipation in  $R_{EUT}$ .** At a minimum, the continuous power rating of resistive elements must nearly equal the actual power dissipation during the longest AC power fault tests. For the short duration, high current stress tests, the actual power dissipation generally exceeds the component's continuous power rating. This is possible in part because the multiple exposure test sequences allow cooling between fault applications effectively resulting in a low duty factor. Unfortunately, it is the usual case that such component "over-rating" factors specific to the test parameters are not available for many parts. If the manufacturer is not able to supply sufficient information, testing may be the only useful means to select parts. Happily, such tests are easy to conduct by breadboarding. It is not necessary to have a complete working line card to collect the necessary information.

A key to the evaluation of  $I^2R$  stress is the determination of the root-mean-square value of the fault current. The non-linear voltage limiting components in the circuit will alter the sinusoidal AC waveshape and complicate the computation of RMS current. Direct True RMS readings may be made – be cautious since the True RMS function on many DMMs is not reliable for waveforms containing fast edges – or the value may be estimated by the methods discussed below.

**Current and power dissipation in zener diode clamps.** Refer to *Figure 12c* below. If the open circuit peak voltage of the fault generator is  $V_{PP}$ , the voltage across one zener at peak reverse current flow is  $V_{PK}^{-1}$ , the voltage across the second zener at peak forward current flow is  $V_{FZ}$ , the series current limiting resistance added by the E.U.T is  $R_{EUT}$  and the generator's output resistance is  $R_{GEN}$ , then the approximate peak surge current for the direction shown<sup>2</sup> is

$$I_{PK} = \frac{V_{PP} - V_{PK} - V_{FZ}}{R_{GEN} + R_{EUT}} \cong \frac{V_{PP} - V_{PK}}{R_{GEN} + R_{EUT}}$$

<sup>1</sup> The ratio of the maximum surge voltage,  $V_{PK}$ , to the nominal zener avalanche voltage is referred to as the clamping factor,  $f_c$ . As a rough and ready rule, use  $f_c = 1.25$  for conditions near the pulse power Watt-second limit. There are two offsetting factors which make this a reasonable assumption. Heating will cause the zener voltage,  $V_Z$ , to rise as the diode is heated at about 0.1% per °C for zeners in the 100 to 200 V range. On the other hand, the dynamic impedance falls with increased junction temperature reducing the  $I_{PK}R$  voltage drop contribution. Data sheets for devices rated for transient protection service frequently include enough surge handling information to verify surge capacity although the information is not always in a convenient form.

<sup>2</sup> The clamping voltages of the zeners may be different in which case the half cycles will have different peak reverse surge voltages and different peak currents, e.g. ( $V_{PK,2}^{-1}, I_{PK,2}^{-1}$ ) and ( $V_{PK,1}^{-1}, I_{PK,1}^{-1}$ ).

Note that, in this application, the  $V_{FZ}$  term is negligible and may be dropped. Until the zener breaks into reverse conduction, the current is essentially zero. Once conduction begins, the current waveform is approximately described by an offset sine function:

$$i(\theta) \cong I_{PP} \cdot \sin(\theta) - I_{OS} \quad \text{where} \quad I_{OS} = I_{PP} - I_{PK} \quad \text{and}$$

$$I_{PP} = I_{PK} \Big|_{V_{PK}=0} = \frac{V_{PP}}{R_{GEN} + R_{EUT}} \quad \text{so that} \quad I_{OS} \cong \frac{V_{PK}}{R_{GEN} + R_{EUT}}$$

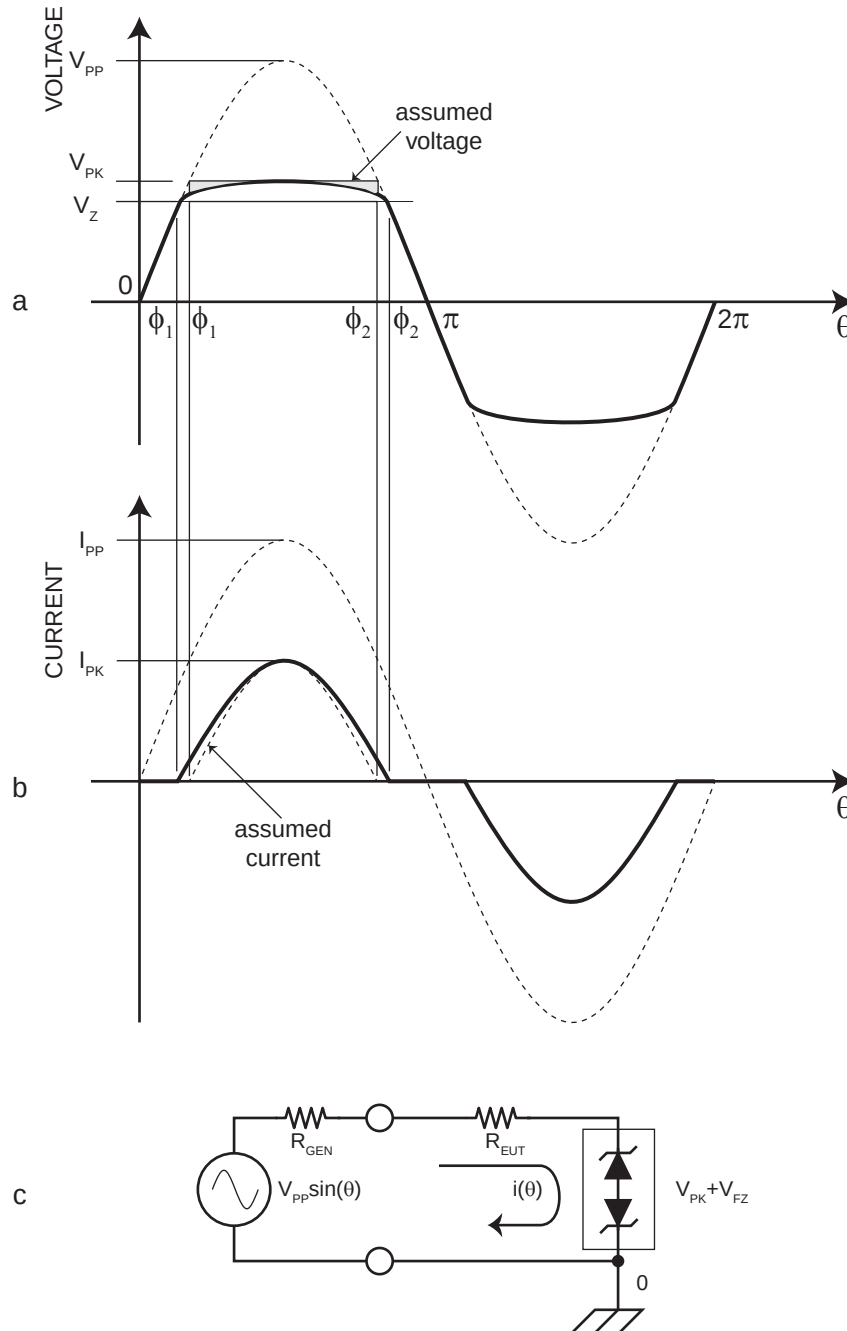


Figure 12 Back to Back Zener Over Voltage Protector Operation



The simplifying assumptions have been made that the voltage across the zener is constant at  $V_{PK}$  during the entire reverse conduction period and that reverse conduction does not occur until the generator voltage exceeds  $V_{PK}$ . Then voltage versus phase function for the first half cycle is expressed

$$v_z(\theta) \cong \begin{cases} 0 \leq \theta < \phi_1 : V_{PP} \sin(\theta) \\ \phi_1 \leq \theta < \phi_2 : V_{PK} \\ \phi_2 \leq \theta < \pi : V_{PP} \sin(\theta) \end{cases}$$

The shaded areas in Figure 12a represent the difference between the assumed and actual zener voltage during reverse conduction. The small amount of power dissipation that would occur for  $\phi_1' \leq \theta < \phi_1$  and for  $\phi_2 < \theta \leq \phi_2'$  is neglected. For the assumed conduction range of  $\phi_1 \leq \theta < \phi_2$ , the overestimation of voltage is roughly balanced by the underestimation of current. Fortunately, the error is smallest when the instantaneous power is the greatest. Additionally, the worst case conditions occur when  $I_{PP} \gg I_{PK}$ , in which case the errors are even less significant. For our purposes, at least, we can comfortably express current as a function of phase during the first half cycle as

$$i(\theta) \cong \begin{cases} 0 \leq \theta < \phi_1 : 0 \\ \phi_1 \leq \theta < \phi_2 : \frac{1}{R_{GEN} + R_{EUT}} [V_{PP} \cdot \sin(\theta) - V_{PK}] \\ \phi_2 \leq \theta < \pi : 0 \end{cases}$$

where

$$\phi_1 = \sin^{-1} \left( \frac{V_{PK}}{V_{PP}} \right) \quad \text{and} \quad \phi_2 = \pi - \sin^{-1} \left( \frac{V_{PK}}{V_{PP}} \right)$$

The instantaneous power dissipation in the zener can then be computed from the  $i \cdot v$  product

$$p_z(\theta) = i(\theta) \cdot v_z(\theta) \cong \begin{cases} 0 \leq \theta < \phi_1 : 0 \\ \phi_1 \leq \theta < \phi_2 : \left[ \frac{V_{PK}}{R_{GEN} + R_{EUT}} \right] \cdot [V_{PP} \cdot \sin(\theta) - V_{PK}] \\ \phi_2 \leq \theta < \pi : 0 \end{cases}$$

This can be then be integrated over the first half cycle to find the average power.

$$P_{Z1} \cong \frac{1}{\pi} \left[ \frac{V_{PK}}{R_{GEN} + R_{EUT}} \right] \cdot \left[ V_{PP} \int_{\phi_1}^{\phi_2} \sin(\theta) d\theta - V_{PK} \int_{\phi_1}^{\phi_2} d\theta \right]$$

The definite integrals may be evaluated as follows.

$$P_{Z1} \cong \frac{1}{\pi} \left[ \frac{V_{PK}}{R_{GEN} + R_{EUT}} \right] \cdot [V_{PP} (-\cos \phi_2 + \cos \phi_1) - V_{PK} \cdot (\phi_2 - \phi_1)]$$

Recall that

$$\phi_2 = \pi - \phi_1, \quad \text{where} \quad \phi_1 = \sin^{-1} \left( \frac{V_{PK}}{V_{PP}} \right),$$

so that

$$\cos(\phi_2) = \cos(\pi - \phi_1) = \cos \pi \cdot \cos \phi_1 + \sin \pi \cdot \sin \phi_1 = -\cos \phi_1$$

Finally

$$P_{Z1} \cong \frac{1}{\pi} \left[ \frac{V_{PK}}{R_{GEN} + R_{EUT}} \right] \cdot [V_{PP} (2 \cdot \cos \phi_1) - V_{PK} \cdot (\pi - 2 \cdot \phi_1)]$$

Power dissipation in the other zener element,  $P_{Z_2}$ , occurring during the second half of the cycle may or may not be the same depending on whether the peak zener voltage for the second diode is the same. If the two diodes are integrated into a single package, the two powers must be calculated separately and then averaged to figure total dissipation for the device. If the two diodes are separate, then the power calculated above may be divided by 2 to account for the average power over both half cycles.

In order to compute the power dissipation in  $R_{EUT}$ , it is necessary to compute the root-mean-square value of  $i(\theta)$ . From the above we have

$i_Z(\theta) \cong I_{PP} \cdot \sin(\theta) - I_{OS}$ , during reverse conduction in the zener. The square of current over the half cycle is

$$i_Z^2(\theta) \cong \begin{cases} 0 \leq \theta < \phi_1 : 0 \\ \phi_1 \leq \theta < \phi_2 : I_{PP}^2 \cdot \sin^2(\theta) - I_{PP} \cdot I_{OS} \cdot \sin(\theta) + I_{OS}^2 \\ \phi_2 \leq \theta < \pi : 0 \end{cases}$$

The root-mean-square current is then

$$I_{RMS} \cong \left[ \frac{1}{\pi} \left( I_{PP}^2 \int_{\phi_1}^{\phi_2} \sin^2(\theta) d\theta - I_{PP} \cdot I_{OS} \int_{\phi_1}^{\phi_2} \sin(\theta) d\theta + I_{OS}^2 \int_{\phi_1}^{\phi_2} d\theta \right) \right]^{\frac{1}{2}}$$

$$I_{RMS} \cong \left[ \frac{1}{\pi} \left( I_{PP}^2 \cdot \frac{1}{2} (\theta - \sin \theta \cdot \cos \theta) \Big|_{\theta=\phi_1}^{\theta=\phi_2} - I_{PP} \cdot I_{OS} (-\cos \phi_2 + \cos \phi_1) + I_{OS}^2 (\phi_2 - \phi_1) \right) \right]^{\frac{1}{2}}$$

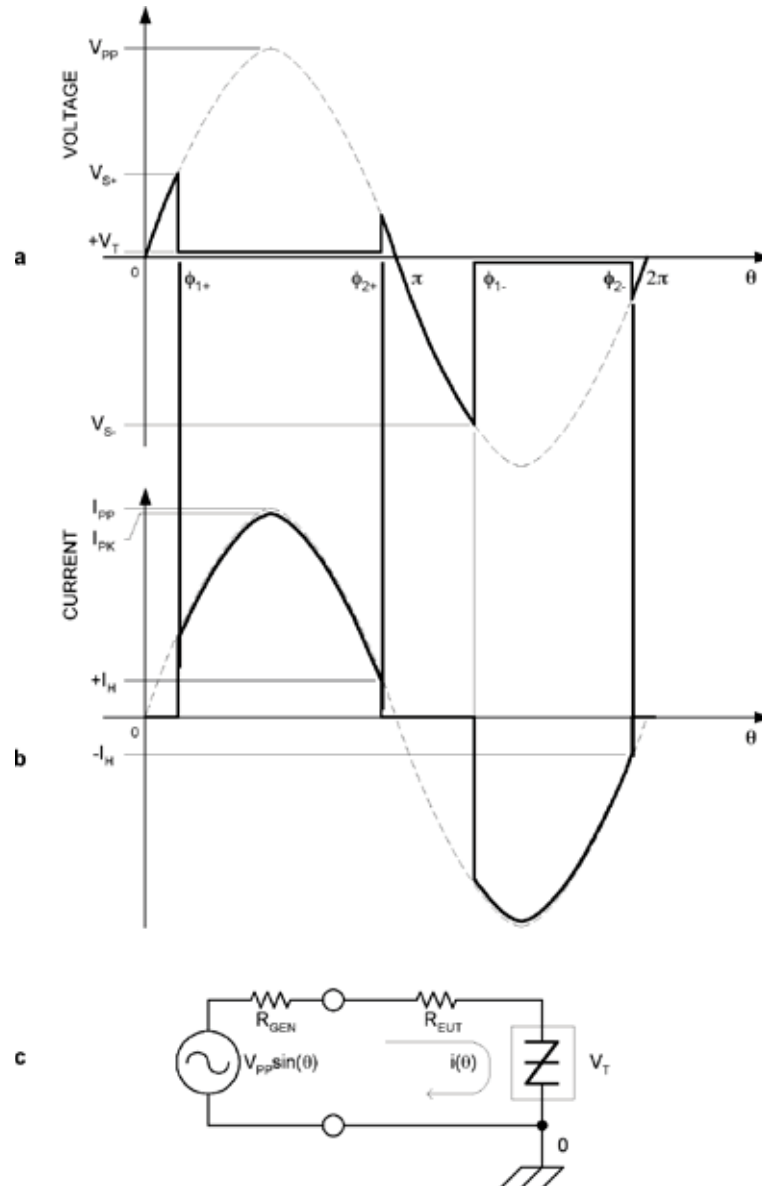
$$I_{RMS} \cong \left[ \frac{1}{\pi} \left( I_{PP}^2 \cdot \left( \frac{\pi}{2} - \phi_1 + \sin \phi_1 \cdot \cos \phi_1 \right) - I_{PP} \cdot I_{OS} (2 \cdot \cos \phi_1) + I_{OS}^2 (\pi - 2 \cdot \phi_1) \right) \right]^{\frac{1}{2}}$$

Once this has been evaluated for a particular set of values, the power dissipated in  $R_{EUT}$  is simply

$$P_{R_{EUT}} = I_{RMS}^2 \cdot R_{EUT}$$

To summarize,

1. The test generator parameters  $V_{PP}$  and  $R_{GEN}$  are extracted from the power fault test description.
2. The proposed circuit parameters  $V_{PK}$  and  $R_{EUT}$  are recorded.
3. These values are used to calculate  $\phi_F$ ,  $I_{PP}$  and  $I_{OS}$ .
4. The equations for  $P_Z$  and  $I_{RMS}$  may now be evaluated.
5. If the zener is
  - part of a back-to-back, dual diode component with symmetric  $V_{PK}$  values, the initial result for  $P_Z$  is correct as it stands;
  - a discrete component, divide  $P_Z$  by 2 to find the power dissipation for the individual part;
  - part of a back-to-back, dual diode component with a different  $V_{PK}$  for the alternate polarity, calculate  $P_Z$  for the second value of  $V_{PK}$  and average the two results.
6.  $P_{R_{EUT}}$  is calculated.
7. If  $V_{PK}$  is
  - symmetric in both directions, the initial result for  $P_{R_{EUT}}$  is correct;
  - asymmetric, calculate  $I_{RMS}$  for the second value of  $V_{PK}$ , compute  $P_{R_{EUT}}$  separately for each current and average the two results.



**Figure 13 Crowbar Type Over Voltage Protector Operation – Asymmetric Thresholds**

Current and power dissipation in foldback or crowbar voltage clamps. The analysis of the zener diode overvoltage protection circuit largely applies to that of the crowbar OVP circuit of Figure 13c above. Unlike the zener circuit, once the conduction threshold is achieved – this occurs at  $V_S$ <sup>1</sup> in the nomenclature of the foldback device – the voltage drop switches to a much lower value,  $V_T$ . Therefore the  $V_{PK}$  (or the comparable  $V_S$ ) term is now replaced by  $V_T$ , the guaranteed maximum on state voltage drop at rated current,  $I_T$ . Again the open circuit peak voltage of the fault generator is  $V_{PP}$ , the series current limiting resistance added by the E.U.T is  $R_{EUT}$  and the generator's output resistance is  $R_{GEN}$ . The approximate peak surge current for the direction shown is

$$I_{PK} \cong \frac{V_{PP} - V_T}{R_{GEN} + R_{EUT}}$$

<sup>1</sup> As remarked under Selecting secondary protection architecture in section 3.2, for lower values of  $V_{PP}$ , a foldback device of the types recommended may behave in manner similar to a zener diode in that they may simply clamp at  $V_S$  until sufficient current flows to achieve switching. Therefore the developed model for power in the OVP device,  $P_{OVP}$ , may be inaccurate at low stress levels.

Again, the current will be essentially zero until break-over and once the device switches into the low impedance on state, the expression for current flow will have the same form. The significant difference is that the current offset term,  $I_{OS}$ , will be far smaller than before since  $V_T \ll V_S$  in this application. This is reflected in the character of the current waveform of *Figure 13b*. There is a large current step as the voltage dropped across  $R_{GEN} + R_{EUT}$  suddenly increases. In fact, for tests where  $V_{PP}$  is much greater than  $V_S$ , the angle of the onset of conduction is relatively small and the magnitude of  $I_{OS}$  is very small compared to  $I_{PP}$  so that a good approximation of current is simply a sine function with amplitude  $I_{PP}$ . More generally, however,

$$i_{OVP}(\theta) \cong I_{PP} \cdot \sin(\theta) - I_{OS} \quad \text{where} \quad I_{OS} = I_{PP} - I_T \cong \frac{V_T}{R_{GEN} + R_{EUT}}$$

The only complication arising from the use of foldback voltage limiters of this type is that the cessation of current flow is a function of current rather than voltage making the angles  $\phi_1$  and  $\phi_2$  independent quantities. These thyristor based devices return to the high impedance off state when current flow falls below the specified hold current,  $I_H$ . So

$$\phi_1 = \sin^{-1} \left( \frac{V_S}{V_{PP}} \right) \quad \text{very much as before while}$$

$$\phi_2 = \pi - \sin^{-1} \left( \frac{I_H}{I_{PK}} \right)$$

Consequently, some of the trigonometric simplifications that were made previously do not apply. Otherwise, the expressions for power in the OVP device and the RMS current can be written out based on the previous solutions using the revised terms.

$$v_{OVP}(\theta) \cong \begin{cases} 0 \leq \theta < \phi_1 : V_{PP} \sin(\theta) \\ \phi_1 \leq \theta < \phi_2 : V_T \\ \phi_2 \leq \theta < \pi : V_{PP} \sin(\theta) \end{cases} \quad \text{and}$$

$$i_{OVP}(\theta) \cong \begin{cases} 0 \leq \theta < \phi_1 : 0 \\ \phi_1 \leq \theta < \phi_2 : \frac{1}{R_{GEN} + R_{EUT}} [V_{PP} \cdot \sin(\theta) - V_T] \\ \phi_2 \leq \theta < \pi : 0 \end{cases} \quad \text{or simply}$$

$$i_{OVP}(\theta) \cong \begin{cases} 0 \leq \theta < \phi_1 : 0 \\ \phi_1 \leq \theta < \phi_2 : I_{PP} \cdot \sin(\theta) - I_{OS} \\ \phi_2 \leq \theta < \pi : 0 \end{cases}$$

The instantaneous current squared during the positive half cycle is again

$$i_{OVP}^2(\theta) \cong \begin{cases} 0 \leq \theta < \phi_1 : 0 \\ \phi_1 \leq \theta < \phi_2 : I_{PP}^2 \cdot \sin^2(\theta) - I_{PP} \cdot I_{OS} \cdot \sin(\theta) + I_{OS}^2 \\ \phi_2 \leq \theta < \pi : 0 \end{cases}$$

Finally, the solutions for the power dissipated in the crowbar protector and the RMS current in the circuit may be written

$$P_{OVP} \cong \frac{1}{\pi} \left[ \frac{V_T}{R_{GEN} + R_{EUT}} \right] \cdot [V_{PP} (-\cos \phi_2 + \cos \phi_1) - V_T \cdot (\phi_2 - \phi_1)]$$

$$I_{RMS} \cong \left[ \frac{1}{\pi} \left( I_{PP}^2 \cdot \frac{1}{2} (\phi_2 - \phi_1 - \sin \phi_2 \cdot \cos \phi_2 + \sin \phi_1 \cdot \cos \phi_1) - I_{PP} \cdot I_{OS} (-\cos \phi_2 + \cos \phi_1) + I_{OS}^2 (\phi_2 - \phi_1) \right) \right]^{\frac{1}{2}}$$

Of course the power dissipated in  $R_{EUT}$  remains

$$P_{R_{EUT}} = I_{RMS}^2 \cdot R_{EUT}$$

Since the crowbar overvoltage protector devices recommended in the LFR Module and the Discrete SMT protection solutions discussed above are already rated by their manufacturers for the application,  $P_{OVP}$  is of little interest to us except to contrast it with  $P_z$  for the same conduction threshold.

On the other hand, being able to calculate the value of  $I_{RMS}$  may be very helpful in sizing components for  $R_{EUT}$  if the part being considered has not already been appropriately rated. This can be even more important when using foldback protectors since the current experienced by  $R_{EUT}$  will be somewhat higher than in a comparable non-foldback circuit. As before, in the event the thresholds of switching operation for positive and negative polarities are different so that

$$V_{S+} \neq V_{S-}$$

which is the case suggested in *Figure 13*, separate calculations for  $I_{RMS}$  must be done for each half cycle. Once that is done, the power dissipation for each half cycle may be calculated and averaged together.

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