Guidelines for Effective LITELINK™ Designs

1. Introduction

Two of the important functions provided by LITELINK to the host systems are high-voltage isolation between the host system and the public switched telephone network (PSTN), and coupling signals to and from the PSTN.

Printed-circuit board layout for LITELINK designs requires attention to detail with regard to these functions. This application note describes design techniques and practices for compliance and performance that should be considered when designing with LITELINK. Examples in this application note are based on a dial-up modem host system, but are applicable to any LITELINK implementation.

Note that some of these guidelines are based on safety requirements for Information Technology Equipment. Designs that must meet other safety requirements may require other considerations.

2. Circuit Isolation Considerations

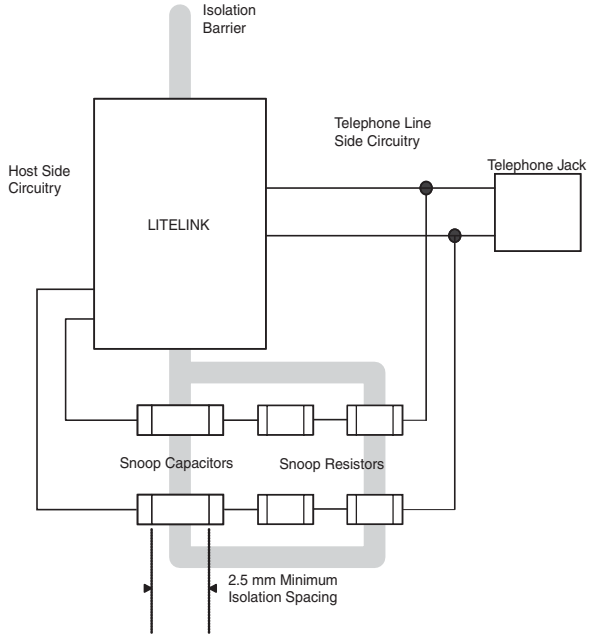
TIA/EIA/IS-968 (formerly FCC part 68) compliance requires testing the integrity of the isolation barrier and the surge immunity of the system. These tests include:

- Leakage test - 1000 V_{rms} applied from tip and ring to ground
- Surge test - 1500 V peak applied from tip and ring to ground

LITELINK provides a minimum 1500 V_{RMS} isolation barrier between host-side circuitry (connected to pins 1 through 16) and telephone-line side circuitry (connected to pins 17-32). Passive discrete components used with LITELINK need to meet electrical isolation requirements as well.

The snoop circuit capacitors in the typical application circuit are examples of passive discrete components used in conjunction with LITELINK that must meet isolation barrier requirements. Other discrete components may also have to meet isolation requirements. If, for example, the circuit uses capacitors from tip and ring to Earth to suppress EMI, these must also meet all the requirements for the snoop capacitors listed below.

Figure 1. Isolation Barrier



2.1 Snoop Capacitor and Circuit Spacing Characteristics for Isolation

The snoop components in Figure 1 are used in LITELINK applications for ring detection and caller ID signal coupling. Snoop components bridge the isolation gap. To meet the requirement for basic insulation, the capacitors must comply with the requirements of IEC384-14: 1993, subclass Y2 or Y4. In areas where supplementary insulation is required, the capacitors must either meet the requirements of IEC384-14: 1993, subclass Y1 for a single capacitor for each circuit, or, when two capacitors are used in series for each circuit, both capacitors must comply with IEC384-14: 1993, subclass Y2 or Y4. Further, in designs using two capacitors in series in each snoop circuit, they must be rated for the total working voltage across the pair and have the same nominal capacitance value.

Isolation spacing must include both printed-circuit board traces and component leads. Figure 1 depicts surface-mount technology (SMT) capacitors with wrap-around leads. All component leads and traces

must maintain a minimum of 2.5 mm (0.1 inch) creepage (where the printed-circuit board Material Group is IIIa/b and the pollution degree is 2) between the telephone-line side and ground or any component or printed-circuit board trace on the host equipment side of the circuit.

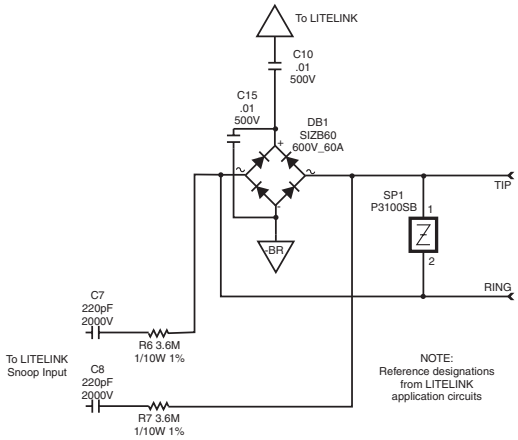
Maintaining this spacing also helps to ensure compliance with the requirements of IEC/EN60950 and UL 1950.

The series resistors in the snoop path may be exposed to high-voltage potentials during transients, so multiple components or resistors with larger terminal spacing may be needed.

2.2 Tip and Ring Spacing Considerations

Similar to isolation barrier requirements, your LITELINK implementation must also account for high-voltage potentials across the tip and ring telephone line leads.

Figure 2. LITELINK Line Side Application Circuit Fragment



Note the surge protection block across the tip and ring leads in Figure 2. This device is normally specified to clamp surge voltages in excess of the maximum ring voltage between tip and ring (metallic surge protection).

Consider an FCC B ring signal. The signal is specified at 150 V_{RMS} maximum, which is 212 Volts peak. Add 100 Volts for loop-extended battery voltage (48 Volts nominal), and the protection device must allow at least 312 Volts before clamping.

The voltage across all components either directly or indirectly across the tip and ring leads can therefor reach well over 300 Volts, up to the clamp rating of the surge protection block. All of the components shown in Figure 2 can have the clamping voltage across them during ringing or a differential surge.

These components be rated accordingly, and the printed-circuit board design must account for these voltages. Maintain at least 1.4 mm (0.055 inch) spacing between all component terminals and adjacent printed-circuit board traces (if the traces are on the same plane) on the telephone line side of the design.

Remember also that all telephone-line-side printed-circuit board traces must maintain at least 2.5 mm (0.1 inch) creepage from all host-equipment-side circuits.

2.3 LITELINK Circuit Isolation Guidelines

- To prevent common-mode noise problems, do not use ground or power printed-circuit board planes in the isolation area. A BR- plane in the isolation area could be used.
- To prevent printed-circuit board trace fusing under surge conditions, maintain a minimum 0.6 mm (0.025 inch) printed-circuit board trace width between the telephone line jack and the surge protection device.
- Observe circuit creepage and clearance requirements per relevant standards, such as UL1950/60950 and IEC/EN60950, and with regard to the insulation grade, working voltage, materials, and pollution degrees involved. For example, if basic insulation is required, and the insulation material group is IIIa/b, and the working voltage does not exceed 100 V_{RMS} or dc, and the pollution degree is 2, then 1.4 mm (0.055 inch) creepage may be required between printed-circuit board traces on the same plane.
- For printed-circuit boards of Material Group IIIa/b and pollution degree 2, maintain minimum creepage of 2.5 mm (0.1 inch) and clearance of 2 mm (0.079 inch) between all circuitry on the high-voltage telephone line side of the printed-circuit board and the low-voltage host equipment side, including grounds. Adjust this spacing for printed-circuit board tolerances.

3. Electro-Magnetic Interference (EMI) Considerations

The telephone line connection in your design can become a source of trouble in meeting EMI

requirements such as FCC part 15. Common origins of EMI in designs that use LITELINK include:

- High-speed clocks
- Poor power supply decoupling
- Poor grounding

3.1 High-Speed Clocks

Your design may include one or more high-speed clock generation circuits, crystals or oscillators. Sharp-edged clock signals can be quite spectrally rich in harmonic energy, making emissions compliance a challenge.

One common way to reduce clock emissions involves adding a small resistance in series with the oscillator output. The resistance, along with parasitic printed-circuit board trace capacitance, can remove enough harmonic energy emission to support compliance.

With this technique, care must be taken not to skew the clock signal so much so as to create timing problems in the system. Resistance values between 10 and 47 Ohms may be enough to meet all requirements. This technique can also be used with microprocessor address, data, and control lines.

Some designs use enough drive for crystal oscillators to cause a significant spectral spike in emissions at the fundamental frequency or one or more harmonics. In these cases, the addition of a small resistor in series with the crystal may help reduce emissions. Consult the crystal manufacturer's product literature for information on applicability of this technique to your design and for suggested series resistor values. If you use this technique, perform all the testing needed to ensure that your oscillator starts and runs under all design temperature condition requirements.

As a general design guide, keep clock and other high-speed signal printed-circuit board traces as short as possible.

3.2 Decoupling

Decoupling system power supplies from oscillator and other noise-generating circuits can help reduce both conducted and radiated emissions.

LITELINK application circuits include a network that provides acceptable power supply decoupling. This network helps prevent coupling power supply noise through LITELINK to the telephone line at frequencies commonly used with switch-mode power supplies.

IXYS IC Division recommends using the inductor variant of the network described in the application circuits if the resistor-based network provides insufficient decoupling. A Pi network using ferrite beads and capacitors can be a better decoupling solution for higher problem frequencies.

In either case, correct placement of the LITELINK power supply decoupling network is vital for an effective design. Place the network as close to the LITELINK VDD and GND pins (pins 1 and 7) as possible.

In general, keep all decoupling circuits as close as possible to the IC being decoupled. Use good-quality tantalum capacitors for bulk decoupling, usually with a value of 10 µF or higher.

There are several useful primers on power supply decoupling on the World Wide Web, including:

- IBM System Board Power Distribution Guidelines for PID9q-604eTM (Mach5)
- Chrontel PCB Layout and Design Considerations for CH7011 TV Output Device
- Altera board layout techniques

3.3 Grounding

For best emission suppression in LITELINK designs, keep analog and digital grounds separate. Analog and digital grounds should be tied together at one point near the power supply.

To reduce ground trace impedance, use printed-circuit board traces at least 1.3 mm (0.050 inch) wide. Group analog and digital circuitry in separate areas where possible.

While ground or power printed-circuit board planes should not be used in the isolated area, the use of a BR- plane in the isolation area is acceptable.

3.4 A LITELINK EMI Filter

Figure 3. LITELINK EMI Filter

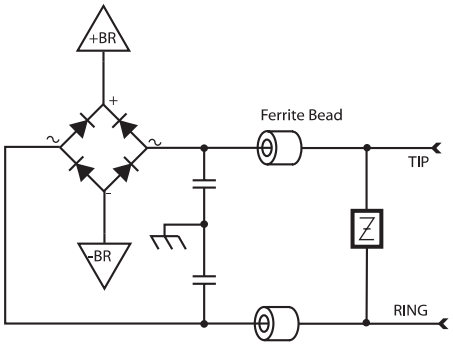


Figure 3 shows an EMI filter than can be applied to LITELINK circuits in conjunction with the standard application circuit in systems using Earth ground. This circuit helps prevent coupling host device emissions to the telephone line.

The capacitors in this circuit must be rated for at least 2 kV, since they are connected to both the telephone line and Earth ground. See Circuit Isolation Considerations on page 2 for more information. Earth ground and host device ground are connected at a single point in the system.

Choose a ferrite with maximum impedance near the frequency of interest. Often, it is difficult to predict the troublesome frequency until you test the system. Failing frequencies are often not the fundamental frequency of the system's clock oscillators, but an n^{th} order harmonic.

Select a ferrite that can accommodate at least 120 mA of current, the maximum steady-state loop current that can be expected on telephone lines. Also, the ferrite must be able to withstand surges without fusing.

Capacitor values will be in the range of several hundred picofarads to one nanofarad. Actual capacitor values will require iterative testing after a good first-order approximation.

4. Heat Management

LITELINKs have low power dissipation and do not need any special design considerations for thermal management. The FET designed and manufactured by IXYS IC Division for use with LITELINK will require heat sinking commensurate with your application. The CPC5602C FET performs three circuit functions:

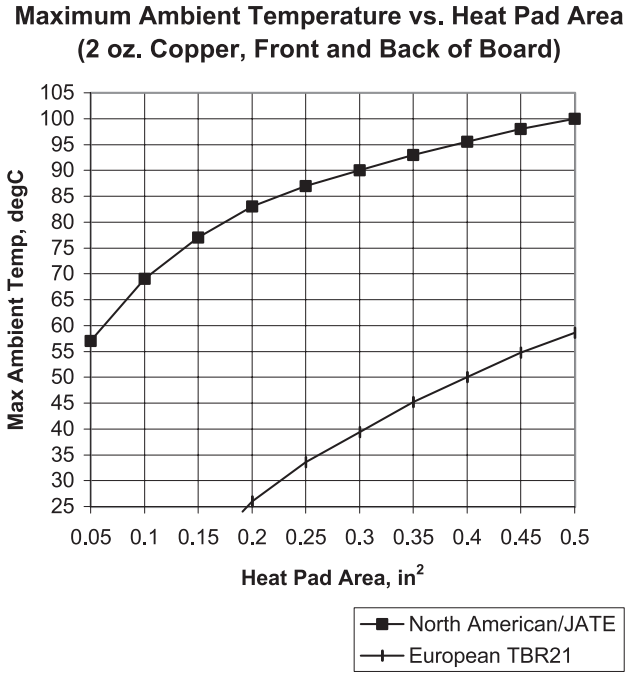
- Low drop-out (LDO) linear regulator
- Unity gain current buffer to the telephone line
- Switchhook

In a TBR-21 application, for example, the FET can be expected to dissipate as much as 2 W of power.

IXYS IC Division suggests incorporating the FET heatsink into your printed-circuit board. Use 2 ounce copper material under the FET heat tab on the other side of the printed-circuit board. Use multiple plated-through holes to conduct heat away from the FET to the heat sink on the other side of the printed-circuit board. For multi-layer printed-circuit board designs, you can also use inner metal layers between the front and back heat pads.

See Figure 4 for heat sink dimension information.

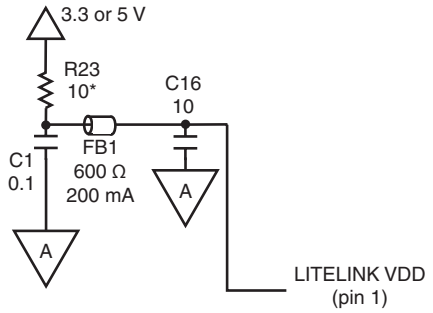
Figure 4. FET Heat Sink Dimensions



5. Power Quality

A clean LITELINK power supply is essential for high-quality connections with LITELINK. LITELINK application circuits include a power conditioning network on VDD to assure clean power.

Figure 5. LITELINK Power Conditioning Network

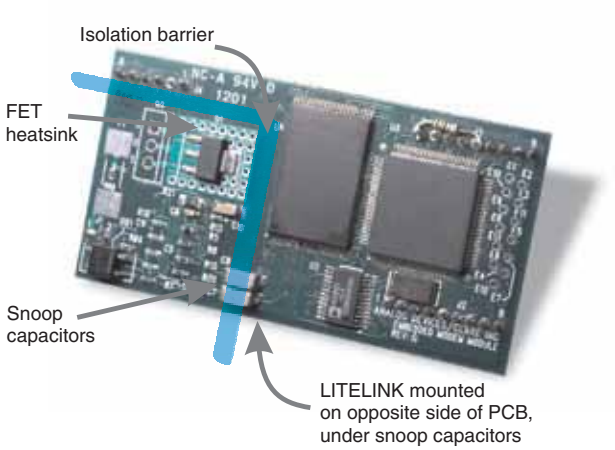


With particularly noisy power supplies, substitute an inductor for R23. IXYS IC Division recommends a value of 220µH in this application, Toko 380HB-2215 or similar.

6. Optimizing LITELINK Circuit Performance

Modem performance is, in part, limited by signal-to-noise ratio (SNR). Careful circuit layout can maximize SNR and provide greater modem throughput.

Figure 6. Modem Design Using LITELINK



In addition to the techniques and guidelines described previously in this application note, consider the following points to optimize your modem design for SNR and performance:

- Use decoupling techniques appropriate for the problem frequency using ferrites and capacitors to form Pi filters in appropriate places.
- Do not use Earth or power planes in the line-side area of your LITELINK implementation printed-circuit board. BR- planes are acceptable.
- Keep the TX +/- and RX +/- line printed-circuit board traces as short as possible. Treat them as differential pairs, running parallel to each other and equidistant.
- Observe isolation barrier requirements when placing snoop circuit and other capacitors connected to tip and ring.
- Treat the snoop circuit lines, including C_{SNOOP} and R_{SNOOP} as a differential pair. Keep printed-circuit board traces as short as possible, parallel and equidistant.
- Keep analog circuitry referenced to analog power and ground. Keep digital circuitry referenced to digital power and ground. Tie analog and digital grounds together at a common point near the power supply.
- Keep FET gate trace lengths as short as possible. For trace lengths longer than IXYS IC Division reference designs, you may want to increase the value of R_{GAT} to assure FET stability. Note: Higher R_{GAT} values increase FET sensitivity to transient events.
- If the design uses a speaker, make sure that the speaker return and audio amplifier return go to analog ground. Also make sure that they have as short as possible a run to power supply ground.
- For audio amplifier (if used) power connections, use the decoupling techniques described in Decoupling on page 4, with the addition of a bulk decoupling capacitor as close as possible to the audio amplifier power supply pin.
- If your design uses an RS-232-type serial port, use ferrite beads in series with the connections to help limit emissions from the port. Consider adding a population option for small 0603-size capacitors from signal lines to analog ground to further diminish emissions, if needed.
- If possible, group the microprocessor, digital signal processor, RAM, and ROM as close together as possible to keep address and data line printed-circuit board traces as short as possible.
- Coder/decoders (CODECs) often have both analog and digital ground connections. Keep these grounds separate. Make sure the LITELINK ground pin connects to analog ground.

7. LITELINK Design Resources

7.1 IXYS IC Division Design Resources

The IXYS IC Division web site has much information useful for designing with LITELINK, including application notes and reference designs that already meet all applicable regulatory requirements. LITELINK data sheets also contains additional application and design information. See the following links:

LITELINK datasheets and reference designs

Application note AN-117 **Customize Caller-ID Gain and Ring Detect Voltage Threshold**

Application note AN-149, **Increased LITELINK II Transmit Power**

For additional information please visit our website at: www.ixysic.com

Specification: AN-146-R03

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