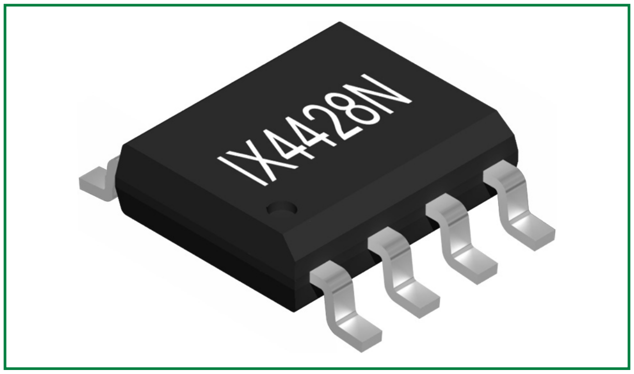
IX4426 / IX4427 / IX4428

1.5 A Dual Low-Side Ultrafast MOSFET Driver



Features

- 1.5 A Peak Output Current
- Wide Operating Voltage Range: 4.5V to 35V
- −40 °C to +125 °C Operating Temperature Range
- Latch-up Protected to 1.5 A
- TTL and CMOS Compatible Inputs
- Ultrafast Rise and Fall Times
- Low Power Consumption

Applications

- MOSFET Driver
- Switching Power Supplies
- Motor Controls
- DC to DC Converters
- Pulse Transformer Driver

Description

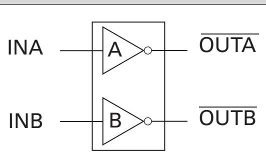
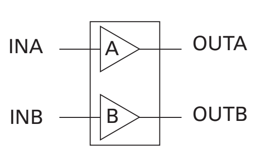
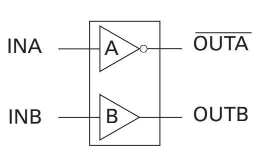
IX4426, IX4427, and IX4428 are dual high-speed, low-side gate drivers. Each of the two outputs can source and sink 1.5 A of peak current and they can switch a 1 nF gate load with rise and fall times of less than 10 ns.

The inputs of each driver are TTL and CMOS compatible, and are virtually immune to latch-up. Low propagation delay times and fast, matched rise and fall times make IX4426, IX4427, and IX4428 ideal for high-frequency and high-power applications.

IX4426 is configured as a dual inverting driver, IX4427 is configured as a dual non-inverting driver, and the IX4428 is configured with one inverting driver and one non-inverting driver.

All three devices are available in a standard 8-pin narrow SOIC package (N suffix), an 8-pin narrow SOIC with an exposed bottom side pad (NE suffix), and an 8-pin DFN package (M suffix).

Ordering Information

Logic Configuration	Part Number	Package Type	Packing Method	Quantity
 INA, INB, A, B, $\overline{OUTA}$, $\overline{OUTB}$	IX4426N	8-Pin Narrow SOIC	Tube	100
	IX4426NTR		Tape and Reel	2000
	IX4426NE	8-Pin Narrow SOIC with exposed Bottom Side Pad	Tube	100
	IX4426NETR		Tape and Reel	2000
	IX4426MTR	8-Pin DFN	Tape and Reel	2000
 INA, INB, A, B, OUTA, OUTB	IX4427N	8-Pin Narrow SOIC	Tube	100
	IX4427NTR		Tape and Reel	2000
	IX4427NE	8-Pin Narrow SOIC with exposed Bottom Side Pad	Tube	100
	IX4427NETR		Tape and Reel	2000
	IX4427MTR	8-Pin DFN	Tape and Reel	2000
 INA, INB, A, B, $\overline{OUTA}$, OUTB	IX4428N	8-Pin Narrow SOIC	Tube	100
	IX4428NTR		Tape and Reel	2000
	IX4428NE	8-Pin Narrow SOIC with exposed Bottom Side Pad	Tube	100
	IX4428NETR		Tape and Reel	2000
	IX4428MTR	8-Pin DFN	Tape and Reel	2000

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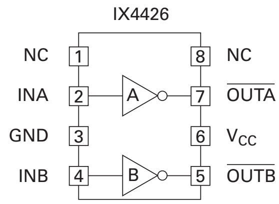
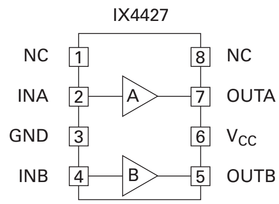
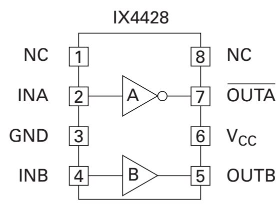
1 Specifications

1.1 Pin Configurations







1.2 Pin Description

Pin Name	Description
INA	Channel A Logic Input
INB	Channel B Logic Input
OUTA or $\overline{\text{OUTA}}$	Channel A Output - Sources or sinks current to turn-on or turn-off a discrete MOSFET or IGBT
OUTB or $\overline{\text{OUTB}}$	Channel B Output - Sources or sinks current to turn-on or turn-off a discrete MOSFET or IGBT
V_{CC}	Supply Voltage - Provides power to the device
GND	Ground - Common ground reference
NC	No connection

1.3 Absolute Maximum Ratings

Parameter	Symbol	Value		Units
		Minimum	Maximum	
Supply Voltage	V_{CC}	–0.3	35	V
Input Voltage	V_{IN}	–5	$V_{CC}+0.3$	V
Output Current	I_{OUT}	—	±1.5	A
Junction Temperature	T_J	–55	+150	°C
Storage Temperature	T_{STG}	–65	+150	°C

Unless otherwise specified, absolute maximum electrical ratings are at 25°C.

Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

1.4 Recommended Operating Conditions

Parameter	Symbol	Value		Units
		Minimum	Maximum	
Supply Voltage	V_{CC}	4.5	30	V
Operating Temperature Range	T_A	–40	+125	°C

1.5 Electrical Characteristics: $T_A = 25°C$

Test Conditions: $4.5V \leq V_{CC} \leq 18V$

Parameter	Conditions	Symbol	Value			Units
			Minimum	Typical	Maximum	
Input Voltage, High	—	V_{IH}	2.4	—	—	V
Input Voltage, Low	—	V_{IL}	—	—	0.8	
Input Current	$0V \leq V_{IN} \leq V_{CC}$	I_{IN}	—	—	±1	μA
Output Voltage, High	—	V_{OH}	$V_{CC} - 0.025$	—	—	V
Output Voltage, Low	—	V_{OL}	—	—	0.025	
Output Resistance, High State	$V_{CC} = 18V$, $I_{OUT} = -100mA$	R_{OH}	—	4	8	Ω
Output Resistance, Low State	$V_{CC} = 18V$, $I_{OUT} = 100mA$	R_{OL}	—	2	4	
Latch-Up Protection	With Reverse Current	I	> 500	—	—	mA
Rise Time	$V_{CC} = 18V$, $C_{LOAD} = 1nF$	t_r	—	10	20	ns
Fall Time		t_f	—	8	20	
On-Time Propagation Delay		t_{on}	—	35	60	
Off-Time Propagation Delay		t_{off}	—	35	60	
Power Supply Current	$V_{INA} = V_{INB} = 3V$	I_{CC}	—	2.5	4	mA
	$V_{INA} = V_{INB} = 0V$		—	0.6	0.8	

1.6 Electrical Characteristics: $T_A = -40°C$ to $+125°C$

Test Conditions: $4.5V \leq V_{CC} \leq 18V$

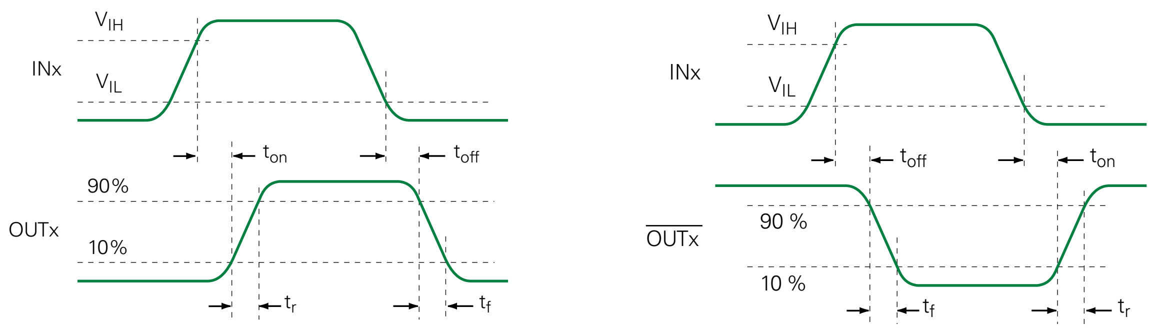
Parameter	Conditions	Symbol	Value		Units
			Minimum	Maximum	
Input Voltage, High	—	V_{IH}	2.4	—	V
Input Voltage, Low	—	V_{IL}	—	0.8	
Input Current	$0V \leq V_{IN} \leq V_{CC}$	I_{IN}	—	±1	μA
Output Voltage, High	—	V_{OH}	$V_{CC} - 0.025$	—	V
Output Voltage, Low	—	V_{OL}	—	0.025	
Output Resistance, High State	$V_{CC} = 18V$, $I_{OUT} = -100mA$	R_{OH}	—	12	Ω
Output Resistance, Low State	$V_{CC} = 18V$, $I_{OUT} = 100mA$	R_{OL}	—	8	
Latch-Up Protection	With Reverse Current	I	> 500	—	mA
Rise Time	$V_{CC} = 18V$, $C_{LOAD} = 1nF$	t_r	—	30	ns
Fall Time		t_f	—	30	
On-Time Propagation Delay		t_{on}	—	70	
Off-Time Propagation Delay		t_{off}	—	70	
Power Supply Current	$V_{INA} = V_{INB} = 3V$	I_{CC}	—	6	mA
	$V_{INA} = V_{INB} = 0V$		—	1	

1.7 Thermal Characteristics

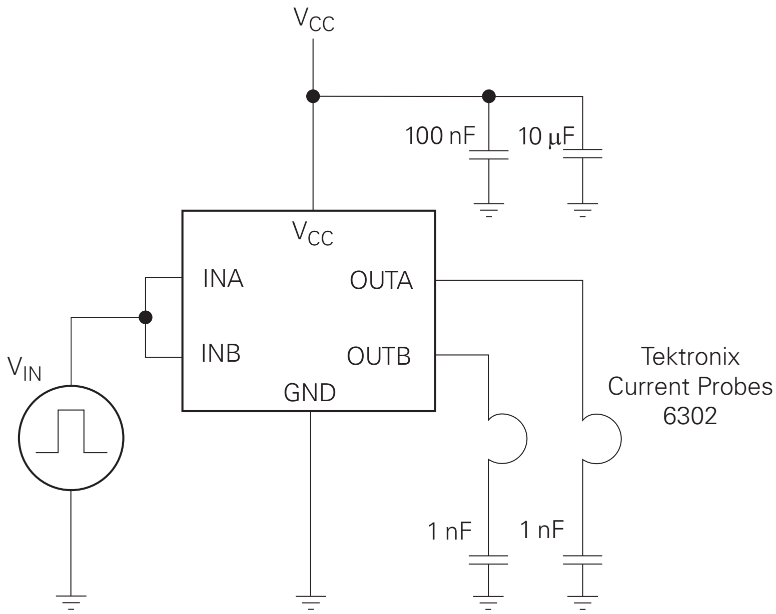
Package	Parameter	Symbol	Rating	Units
8-Pin SOIC with Exposed Bottom Side Pad	Thermal Impedance, Junction to Ambient	θ_{JA}	58	K/W
8-Pin SOIC with Exposed Bottom Side Pad	Thermal Impedance, Junction to Case	θ_{JC}	10	
8-Pin SOIC	Thermal Impedance, Junction to Ambient	θ_{JA}	120	
8-Pin DFN	Thermal Impedance, Junction to Ambient	θ_{JA}	68	
8-Pin DFN	Thermal Impedance, Junction to Case	θ_{JC}	3.73	

2 IX4426 / IX4427 / IX4428 Performance

2.1 Timing Diagram

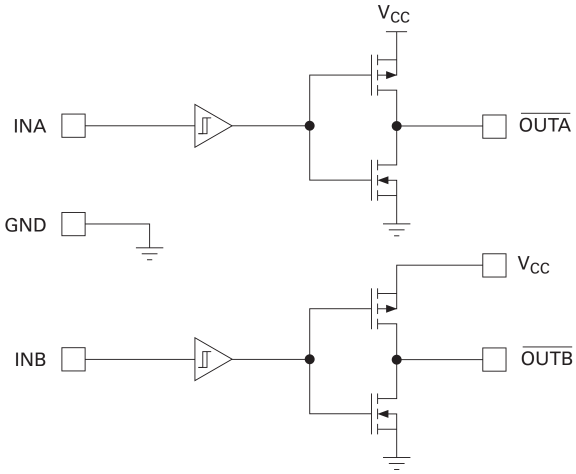


2.2 Characteristics Test Diagrams



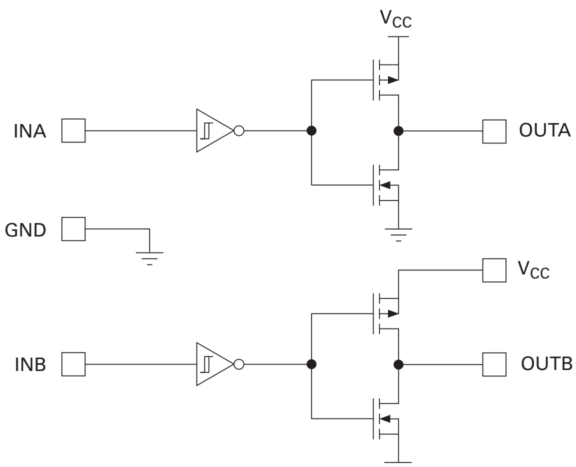
3 Block Diagrams and Truth Tables

3.1 IX4426



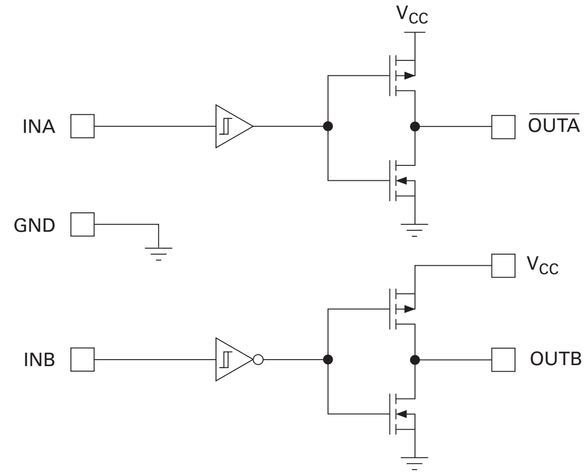
INx	$\overline{OUTx}$
0	1
1	0

3.2 IX4427



INx	$\overline{OUTx}$
0	0
1	1

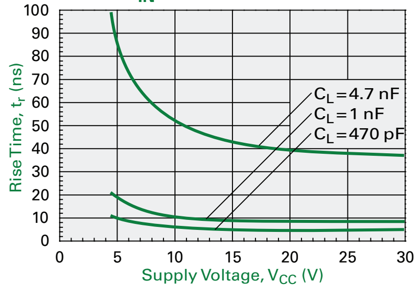
3.3 IX4428



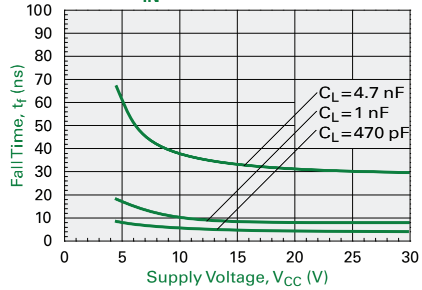
INA	$\overline{OUTA}$
0	1
1	0
INB	**OUTB**
0	0
1	1

4 Performance Data

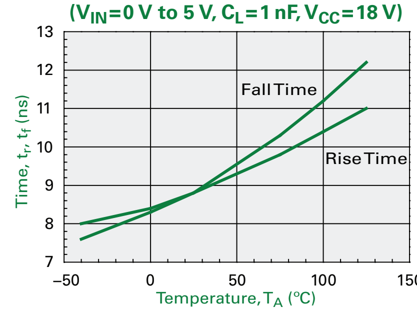
Rise Time vs. Supply Voltage (V_{IN}=0 V to 5 V, f=1 kHz)



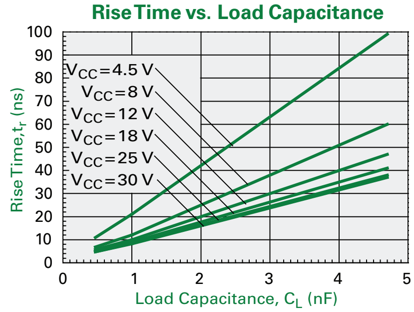
Fall Time vs. Supply Voltage (V_{IN}=0 V to 5 V, f=1 kHz)



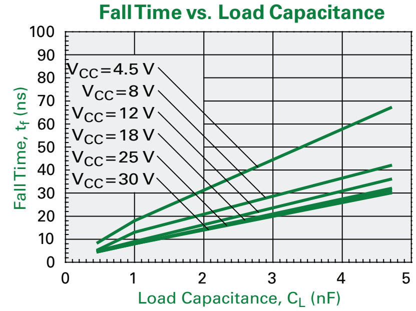
Rise Time and Fall Time vs. Temperature (V_{IN}=0 V to 5 V, C_L=1 nF, V_{CC}=18 V)



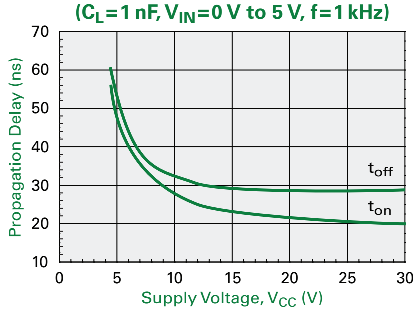
Rise Time vs. Load Capacitance



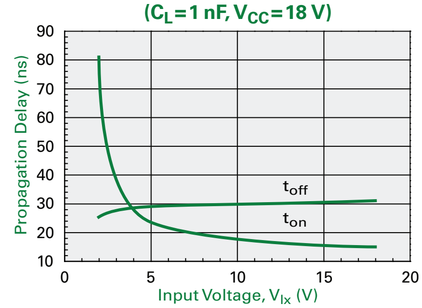
Fall Time vs. Load Capacitance



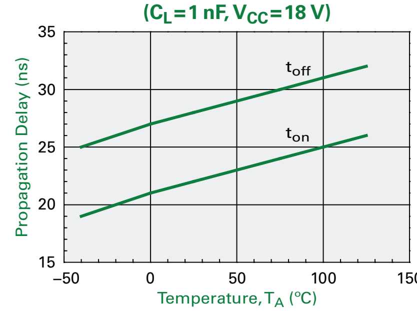
Propagation Delay vs. Supply Voltage (C_L=1 nF, V_{IN}=0 V to 5 V, f=1 kHz)



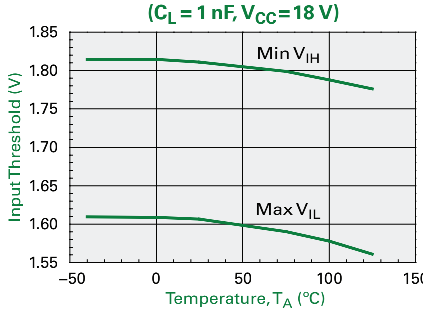
Propagation Delay vs. Input Voltage (C_L=1 nF, V_{CC}=18 V)



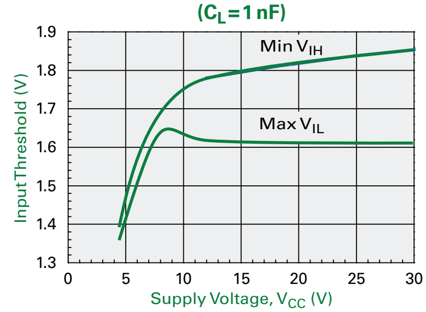
Propagation Delay vs. Temperature (C_L=1 nF, V_{CC}=18 V)



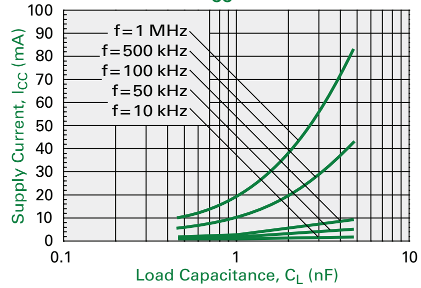
Input Threshold vs. Temperature (C_L = 1 nF, V_{CC}=18 V)



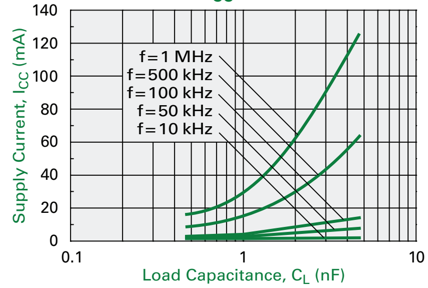
Input Threshold vs. Supply Voltage (C_L=1 nF)



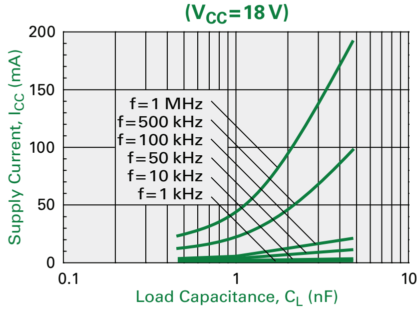
Supply Current vs. Load Capacitance
Both Outputs Active
(V_{CC}=8 V)



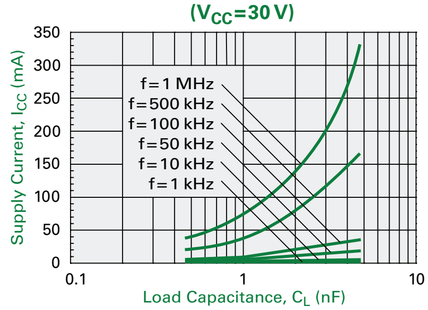
Supply Current vs. Load Capacitance
Both Outputs Active
(V_{CC}=12 V)



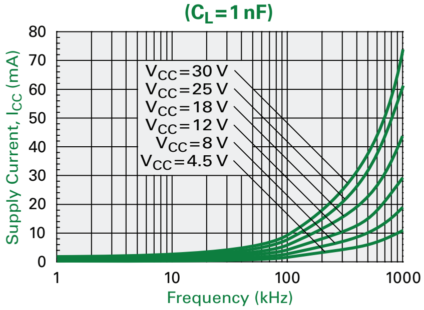
Supply Current vs. Load Capacitance
Both Outputs Active
(V_{CC}=18 V)



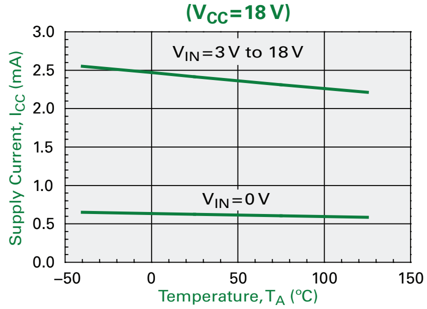
Supply Current vs. Load Capacitance
Both Outputs Active
(V_{CC}=30 V)



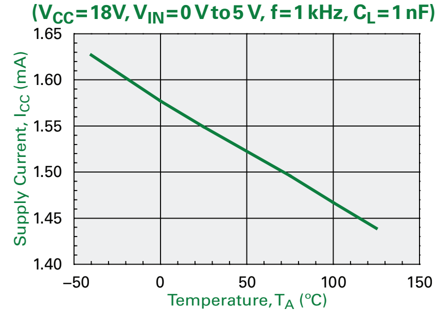
Supply Current vs. Frequency
Both Outputs Active
(C_L=1 nF)



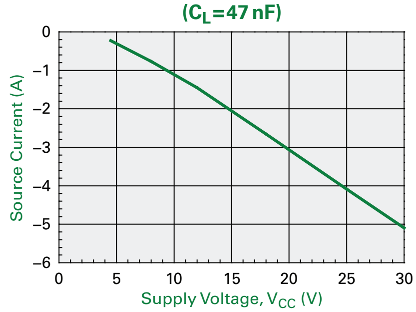
Quiescent Supply Current
vs. Temperature
(V_{CC}=18 V)



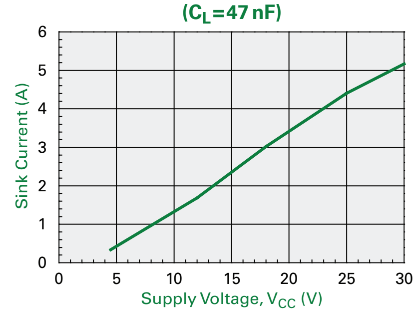
Dynamic Supply Current vs. Temperature
Both Outputs Active
(V_{CC}=18V, V_{IN}=0 V to 5 V, f=1 kHz, C_L=1 nF)



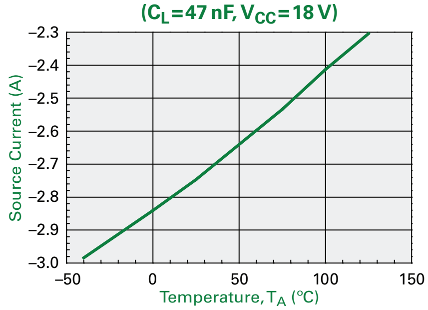
Output Source Current
vs. Supply Voltage
(C_L=47 nF)



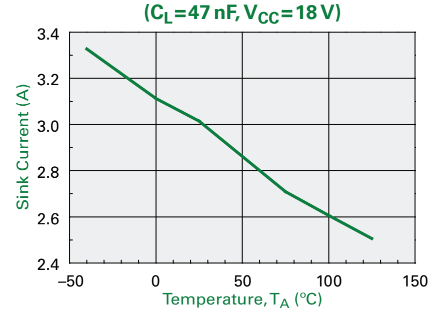
Output Sink Current
vs. Supply Voltage
(C_L=47 nF)



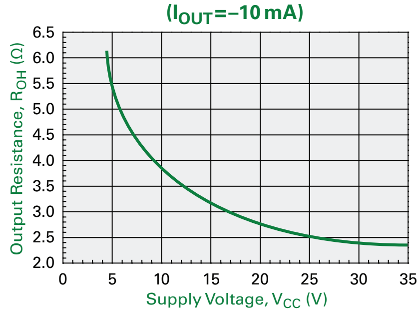
Output Source Current vs. Temperature (C_L=47 nF, V_{CC}=18 V)



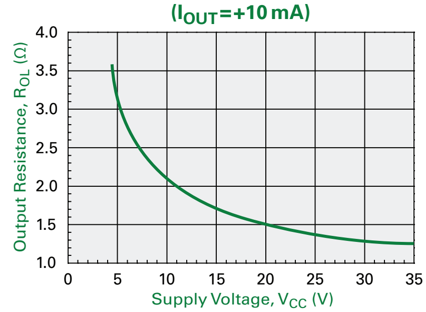
Output Sink Current vs. Temperature (C_L=47 nF, V_{CC}=18 V)



High-State Output Resistance vs. Supply Voltage (I_{OUT}=−10 mA)



Low-State Output Resistance vs. Supply Voltage (I_{OUT}=+10 mA)



5 Manufacturing Information

5.1 Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. Littelfuse classifies its plastic encapsulated devices for moisture sensitivity according to the latest revision of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL)** classification as shown below, and should be handled according to the requirements of the latest revision of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Classification
IX4426 / IX4427 / IX4428, all versions	MSL 1

5.2 ESD Sensitivity

This product is ESD Sensitive, and should be handled according to the industry standard **JESD-625**.

5.3 Soldering Profile

Provided in the table below is the **IPC/JEDEC J-STD-020** Classification Temperature (T_C) and the maximum dwell time (T_C – 5°C). The Classification Temperature sets the Maximum Body Temperature allowed for these devices during reflow soldering processes.

Device	Classification Temperature (T_C)	Dwell Time (t_P)	Maximum Reflow Cycles
IX4426 / IX4427 / IX4428, all versions	260°C	30 seconds	3

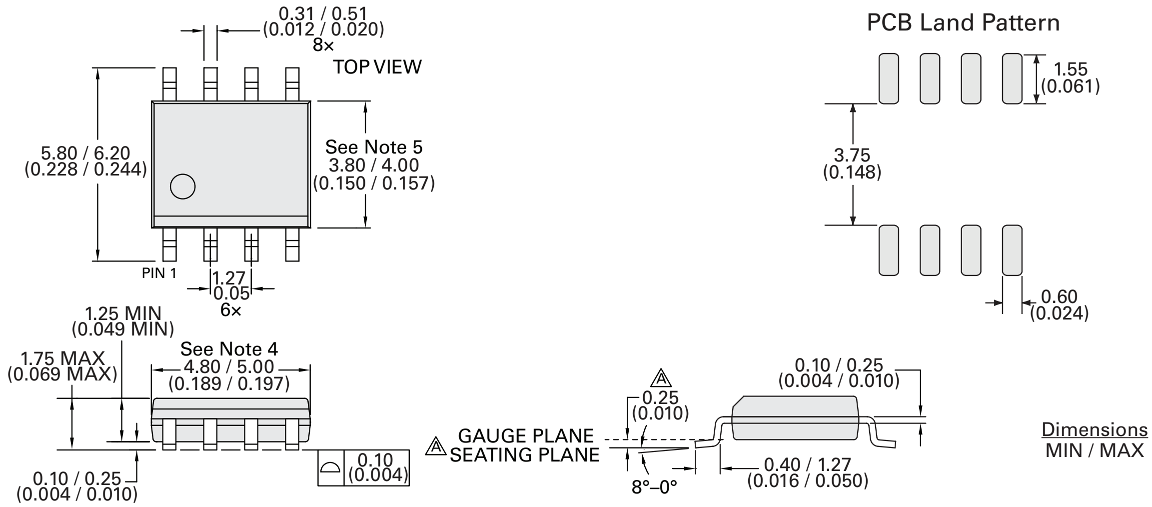
5.4 Board Wash

Littelfuse recommends the use of no-clean flux formulations. Board washing to reduce, or remove flux residue following the solder reflow process is acceptable, provided proper precautions are taken to prevent damage to the device. These precautions include, but are not limited to: Using a low pressure wash and providing a follow-up bake cycle sufficient to remove any moisture trapped within the device, due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning, or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to halide flux or solvents.

Pb RoHS e3

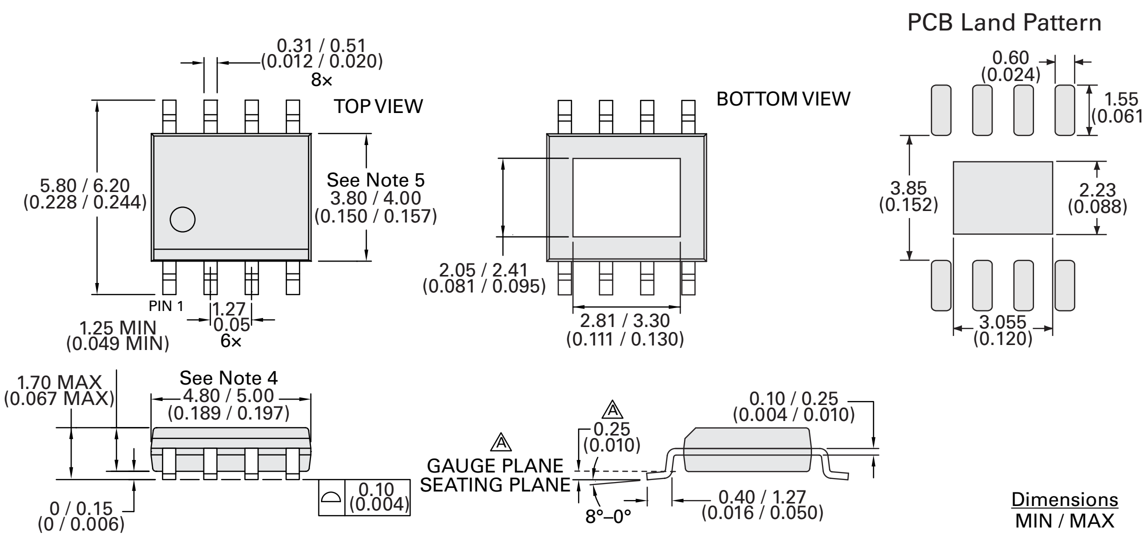
5.5 Mechanical Dimensions

5.5.1 "N" Package (8-Pin Narrow SOIC)



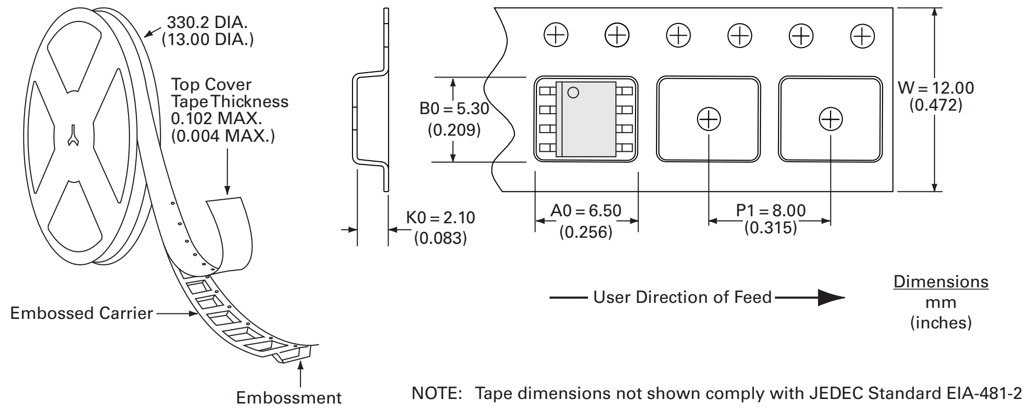
Notes:
1. Controlling dimension: millimeters.
2. All dimensions are in mm (inches).
3. This package conforms to JEDEC Standard MS-012, variation AA, Rev. F.
4. Dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per end.
5. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 mm per side.
6. Lead thickness includes plating.

5.5.2 "NE" Package (8-Pin Narrow SOIC with Exposed Bottom-Side Pad)

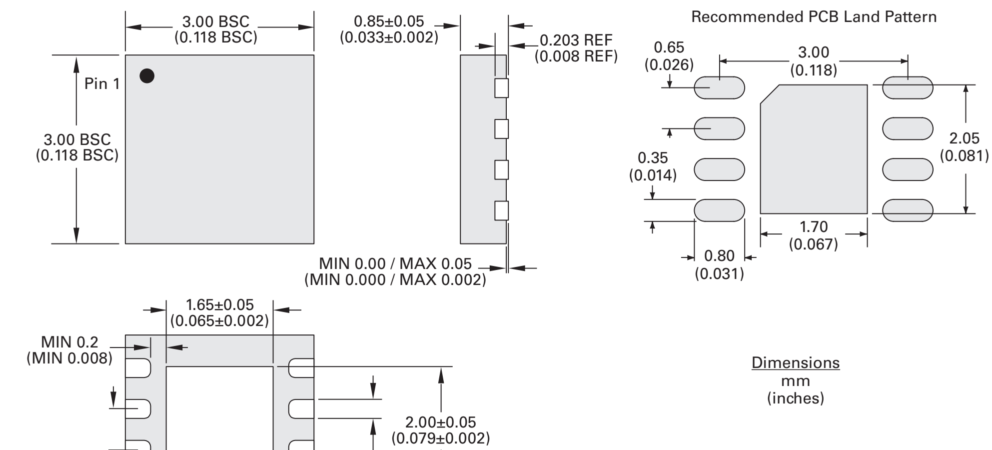


Notes:
1. Controlling dimension: millimeters.
2. All dimensions are in mm (inches).
3. This package conforms to JEDEC Standard MS-012, variation BA, Rev. F.
4. Dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per end.
5. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 mm per side.
6. The exposed metal pad on the back of the package should be connected to GND. It is not suitable for carrying current.
7. Lead thickness includes plating.

5.5.3 "N" and "NE" Package Tape and Reel

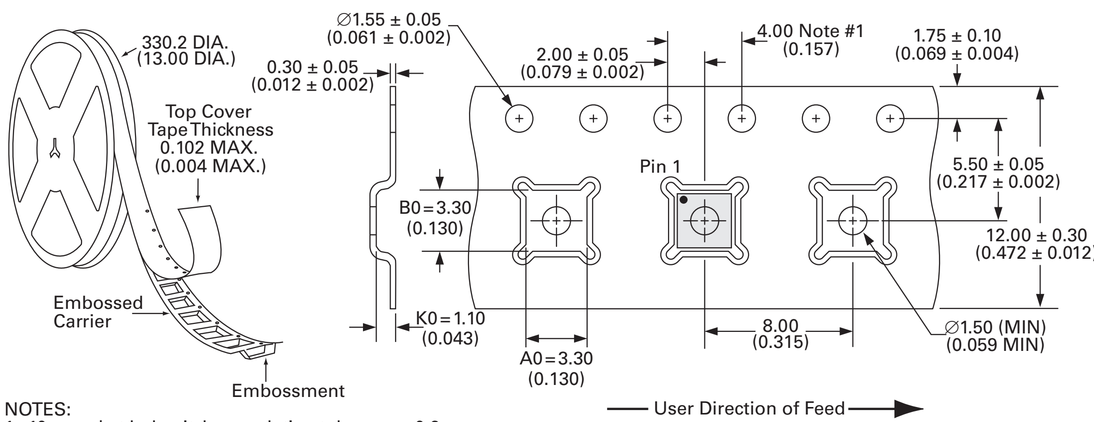


5.5.4 "M" Package (8-Pin DFN)



NOTES:
1. The exposed metal pad on the back of the package should be connected to GND. Pad is not suitable for carrying current.
2. Terminal width (0.30 ± 0.05) mm is measured between 0.15 mm and 0.30 mm from the terminal tip.
3. Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.

5.5.5 "M" Package Tape and Reel



NOTES:
1. 10 sprocket hole pitch cumulative tolerance ±0.2 mm
2. Camber not to exceed 1 mm in 100 mm
3. Material black Advantek Polystyrene
4. A0 and B0 measured on a plane 0.3 mm above the bottom of the pocket
5. K0 measured from a plane on the inside bottom of the pocket to the top surface of the carrier
6. Pocket position relative to the sprocket hole measured as true position of pocket, not pocket hole
7. Cover tape width (9.3±0.1) mm