



High Voltage Thyristor \ Diode Module

$V_{RRM} = 2 \times 2200 \text{ V}$

$I_{TAV} = 150 \text{ A}$

$V_T = 1.18 \text{ V}$

Phase leg

Part number

MCNA150PD2200YB



Backside: isolated



Features / Advantages:

- Thyristor for line frequency
- Planar passivated chip
- Long-term stability

Applications:

- Line rectifying 50/60 Hz
- Softstart AC motor control
- DC Motor control
- Power converter
- AC power control
- Lighting and temperature control

Package: Y4

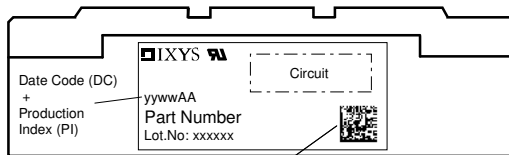
- Isolation Voltage: 4800 V~
- Industry standard outline
- RoHS compliant
- Soldering pins for PCB mounting
- Base plate: DCB ceramic
- Reduced weight
- Advanced power cycling

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Rectifier			Ratings			
Symbol	Definition	Conditions	min.	typ.	max.	Unit
$V_{RSM/DSM}$	max. non-repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}C$			2300	V
$V_{RRM/DRM}$	max. repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}C$			2200	V
I_{RD}	reverse current, drain current	$V_{R/D} = 2200\text{ V}$	$T_{VJ} = 25^{\circ}C$		400	μA
		$V_{R/D} = 2200\text{ V}$	$T_{VJ} = 125^{\circ}C$		15	mA
V_T	forward voltage drop	$I_T = 150\text{ A}$	$T_{VJ} = 25^{\circ}C$		1.24	V
		$I_T = 300\text{ A}$			1.48	V
		$I_T = 150\text{ A}$	$T_{VJ} = 125^{\circ}C$		1.18	V
		$I_T = 300\text{ A}$			1.51	V
I_{TAV}	average forward current	$T_C = 85^{\circ}C$	$T_{VJ} = 140^{\circ}C$		150	A
$I_{T(RMS)}$	RMS forward current	180° sine			235	A
V_{T0}	threshold voltage	} for power loss calculation only	$T_{VJ} = 140^{\circ}C$		0.86	V
r_T	slope resistance				2.1	m Ω
R_{thJC}	thermal resistance junction to case				0.21	K/W
R_{thCH}	thermal resistance case to heatsink			0.11		K/W
P_{tot}	total power dissipation		$T_C = 25^{\circ}C$		550	W
I_{TSM}	max. forward surge current	$t = 10\text{ ms}; (50\text{ Hz}), \text{ sine}$	$T_{VJ} = 45^{\circ}C$		4.30	kA
		$t = 8,3\text{ ms}; (60\text{ Hz}), \text{ sine}$	$V_R = 0\text{ V}$		4.65	kA
		$t = 10\text{ ms}; (50\text{ Hz}), \text{ sine}$	$T_{VJ} = 140^{\circ}C$		3.66	kA
		$t = 8,3\text{ ms}; (60\text{ Hz}), \text{ sine}$	$V_R = 0\text{ V}$		3.95	kA
I^2t	value for fusing	$t = 10\text{ ms}; (50\text{ Hz}), \text{ sine}$	$T_{VJ} = 45^{\circ}C$		92.5	kA ² s
		$t = 8,3\text{ ms}; (60\text{ Hz}), \text{ sine}$	$V_R = 0\text{ V}$		89.8	kA ² s
		$t = 10\text{ ms}; (50\text{ Hz}), \text{ sine}$	$T_{VJ} = 140^{\circ}C$		66.8	kA ² s
		$t = 8,3\text{ ms}; (60\text{ Hz}), \text{ sine}$	$V_R = 0\text{ V}$		64.7	kA ² s
C_J	junction capacitance	$V_R = 700\text{ V}$ $f = 1\text{ MHz}$	$T_{VJ} = 25^{\circ}C$		113	pF
P_{GM}	max. gate power dissipation	$t_p = 30\text{ }\mu s$	$T_C = 140^{\circ}C$		120	W
		$t_p = 300\text{ }\mu s$			60	W
P_{GAV}	average gate power dissipation				8	W
$(di/dt)_{cr}$	critical rate of rise of current	$T_{VJ} = 140^{\circ}C; f = 50\text{ Hz}$ repetitive, $I_T = 450\text{ A}$			150	A/ μs
		$t_p = 200\text{ }\mu s; di_G/dt = 0.5\text{ A}/\mu s;$ $I_G = 0.5\text{ A}; V = \frac{2}{3} V_{DRM}$ non-repet., $I_T = 150\text{ A}$			500	A/ μs
$(dv/dt)_{cr}$	critical rate of rise of voltage	$V = \frac{2}{3} V_{DRM}$ $R_{GK} = \infty; \text{ method 1 (linear voltage rise)}$	$T_{VJ} = 140^{\circ}C$		1000	V/ μs
V_{GT}	gate trigger voltage	$V_D = 6\text{ V}$	$T_{VJ} = 25^{\circ}C$		2	V
			$T_{VJ} = -40^{\circ}C$		2.6	V
I_{GT}	gate trigger current	$V_D = 6\text{ V}$	$T_{VJ} = 25^{\circ}C$		150	mA
			$T_{VJ} = -40^{\circ}C$		200	mA
V_{GD}	gate non-trigger voltage	$V_D = \frac{2}{3} V_{DRM}$	$T_{VJ} = 140^{\circ}C$		0.2	V
I_{GD}	gate non-trigger current				10	mA
I_L	latching current	$t_p = 30\text{ }\mu s$	$T_{VJ} = 25^{\circ}C$		200	mA
		$I_G = 0.45\text{ A}; di_G/dt = 0.45\text{ A}/\mu s$				
I_H	holding current	$V_D = 6\text{ V}$ $R_{GK} = \infty$	$T_{VJ} = 25^{\circ}C$		200	mA
t_{gd}	gate controlled delay time	$V_D = \frac{1}{2} V_{DRM}$	$T_{VJ} = 25^{\circ}C$		2	μs
		$I_G = 0.5\text{ A}; di_G/dt = 0.5\text{ A}/\mu s$				
t_q	turn-off time	$V_R = 100\text{ V}; I_T = 150\text{ A}; V = \frac{2}{3} V_{DRM}$ $di/dt = 10\text{ A}/\mu s$ $dv/dt = 20\text{ V}/\mu s$ $t_p = 200\text{ }\mu s$	$T_{VJ} = 125^{\circ}C$		200	μs

Package Y4				Ratings			
Symbol	Definition	Conditions	min.	typ.	max.	Unit	
I_{RMS}	RMS current	per terminal			300	A	
T_{VJ}	virtual junction temperature		-40		140	°C	
T_{op}	operation temperature		-40		125	°C	
T_{stg}	storage temperature		-40		125	°C	
Weight					150	g	
M_D	mounting torque		2.25		2.75	Nm	
M_T	terminal torque		4.5		5.5	Nm	
$d_{Spp/APP}$	creepage distance on surface striking distance through air	terminal to terminal	14.0	10.0		mm	
$d_{Spb/APb}$		terminal to backside	16.0	16.0		mm	
V_{ISOL}	isolation voltage	t = 1 second	50/60 Hz, RMS; $I_{ISOL} \leq 1$ mA	4800		V	
		t = 1 minute		4000		V	



Data Matrix: part no. (1-19), DC + PI (20-25), lot.no.# (26-31), blank (32), serial no.# (33-36)

Part description

M = Module
 C = Thyristor (SCR)
 N = High Voltage Thyristor
 A = (≥ 2000 V)
 150 = Current Rating [A]
 PD = Phase leg
 2200 = Reverse Voltage [V]
 YB = Y4-M6

Ordering	Ordering Number	Marking on Product	Delivery Mode	Quantity	Code No.
Standard	MCNA150PD2200YB	MCNA150PD2200YB	Box	6	524568

Similar Part	Package	Voltage class
MCNA180PD2200YB	Y4-M6	2200
MCNA220PD2200YB	Y4-M6	2200

Equivalent Circuits for Simulation

* on die level

$T_{VJ} = 140^\circ\text{C}$



Thyristor

$V_{0\ max}$	threshold voltage	0.86	V
$R_{0\ max}$	slope resistance *	1.49	mΩ



Outlines Y4



Dim.	MIN [mm]	MAX [mm]	MIN [inch]	MAX [inch]
a	30.0	30.6	1.181	1.205
b	typ. 0.25		typ. 0.010	
c	64.0	65.0	2.520	2.559
d	6.5	7.0	0.256	0.275
e	4.9	5.1	0.193	0.201
f	28.6	29.2	1.126	1.150
g	7.3	7.7	0.287	0.303
h	93.5	94.5	3.681	3.720
i	79.5	80.5	3.130	3.169
j	4.8	5.2	0.189	0.205
k	33.4	34.0	1.315	1.339
l	16.7	17.3	0.657	0.681
m	22.7	23.3	0.894	0.917
n	22.7	23.3	0.894	0.917
o	14.0	15.0	0.551	0.591
p	typ. 10.5		typ. 0.413	
r	1.8	2.4	0.071	0.041

Optional accessories for modules
Keyed gate/cathode twin plugs with wire length = 350 mm, gate = white, cathode = red
Type ZY 180L (L = Left for pin pair 4/5) UL 758, style 3751



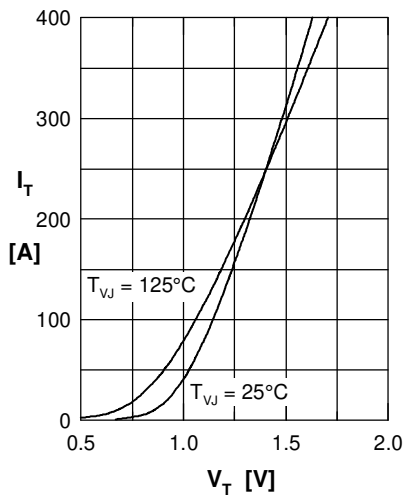
Thyristor


Fig. 1 Forward characteristics

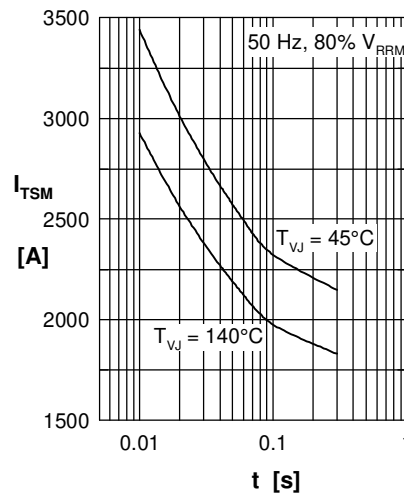
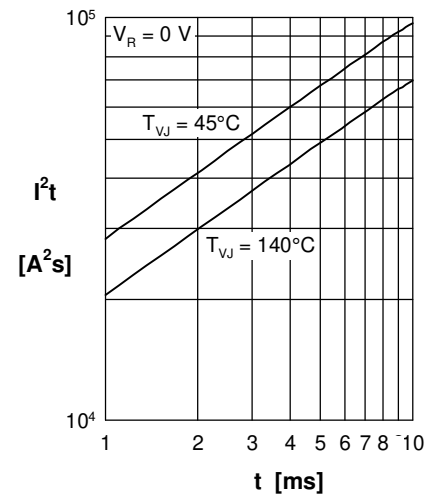
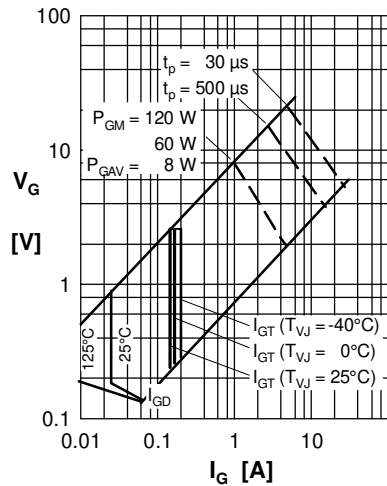

 Fig. 2 Surge overload current
 I_{TSM} : crest value, t : duration

 Fig. 3 I^2t versus time (1-10 s)


Fig. 4 Gate voltage & gate current

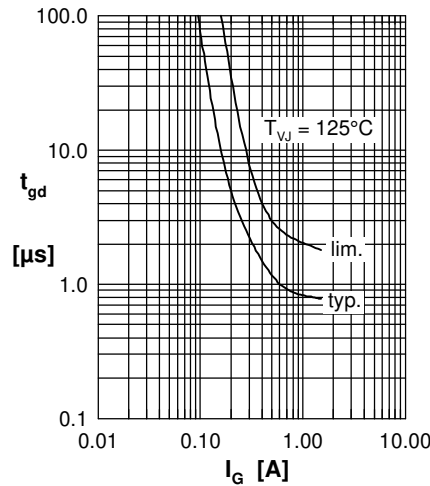
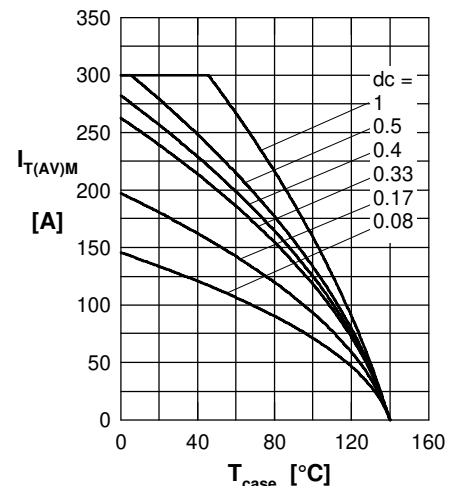

 Fig. 5 Gate controlled delay time t_{gd}


Fig. 6 Max. forward current at case temperature

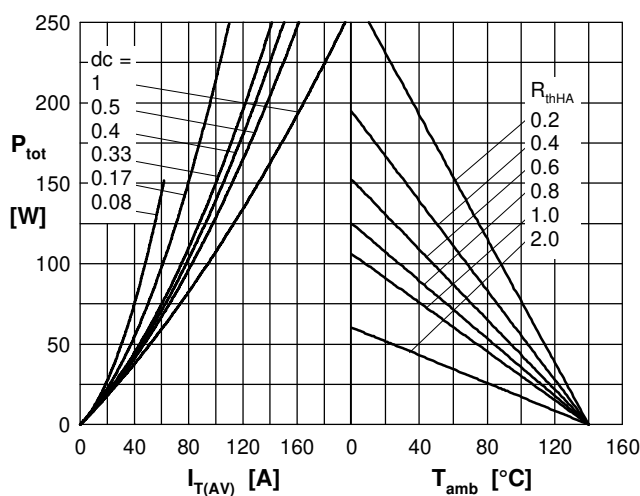
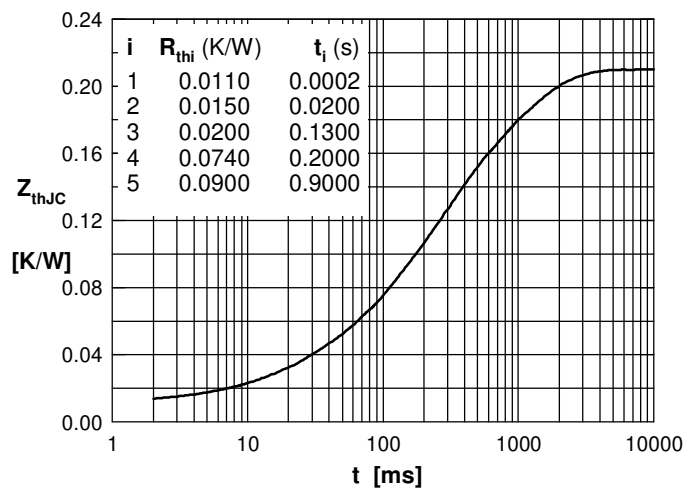

 Fig. 7a Power dissipation versus direct output current
 Fig. 7b and ambient temperature


Fig. 8 Transient thermal impedance junction to case