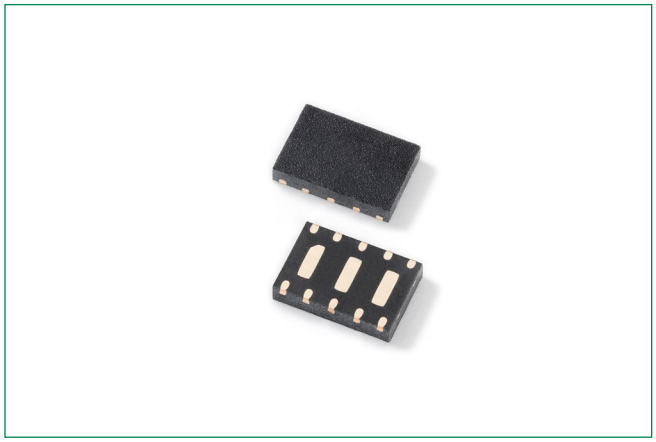
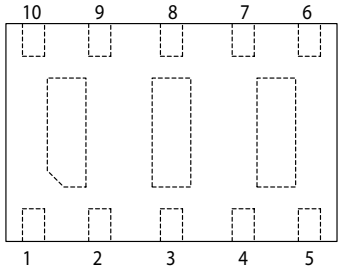
SP2555NUTG Series

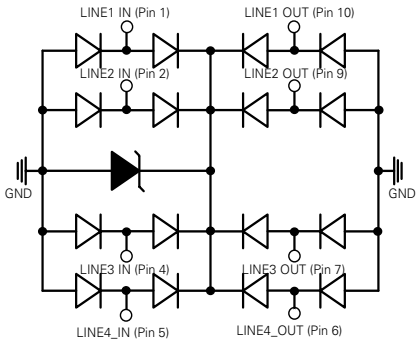
Lightning Surge Protection



Pinout



Functional Block Diagram



Description

The SP2555NUTG is a low-capacitance, TVS Diode Array designed to provide protection against ESD (electrostatic discharge), CDE (cable discharge events), EFT (electrical fast transients), and lightning induced surges for high-speed, differential data lines. It's packaged in a µDFN package (3.0 x 2.0mm) and each component can protect up 4 channels or 2 differential pairs, up to 45A (IEC 61000-4- 5 2nd edition,) and up to 30kV ESD (IEC 61000-4-2). The "flow-through" design minimizes signal distortion, reduces voltage overshoot, and provides a simplified PCB design.

The SP2555NUTG with its low capacitance and low clamping voltage makes it ideal for high-speed data interfaces such as 1GbE applications found in notebooks, switches, etc.

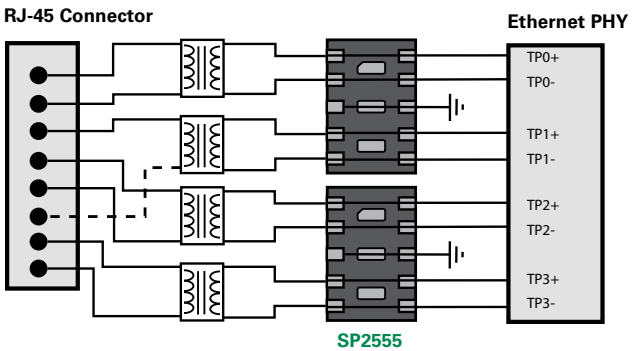
Features & Benefits

- ESD, IEC 61000-4-2, ±30kV contact, ±30kV air
- EFT, IEC 61000-4-4, 40A (5/50ns)
- Lightning, IEC 61000-4-5 2nd Edition, 45A (8/20µs)
- Low capacitance of 2.5pF@0V (TYP) per I/O
- Low leakage current of 0.1µA (TYP) at 2.5V
- µDFN-10 package is optimized for high-speed data line routing
- Provides protection for two differential data pairs (4 channels) up to 45A
- Low operating and clamping voltage
- AEC-Q101 qualified
- Halogen free, Lead free and RoHS compliant

Applications

- 10/100/1000 Ethernet
- WAN/LAN Equipment
- Desktops, Servers and Notebooks
- LVDS Interfaces
- Integrated Magnetics
- Smart TV

Application Example



Life Support Note:

Not Intended for Use in Life Support or Life Saving Applications

The products shown herein are not designed for use in life sustaining or life saving applications unless otherwise expressly indicated.

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Absolute Maximum Ratings

Symbol	Parameter	Value	Units
I_{PP}	Peak Current (t_p=8/20µs)	45	A
P_{Pk}	Peak Pulse Power (t_p=8/20µs)	1000	W
T_{OP}	Operating Temperature	-40 to 125	°C
T_{STOR}	Storage Temperature	-55 to 150	°C

Caution: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the component. This is a stress only rating and operation of the component at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Characteristics (T_{OP}=25°C)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reverse Standoff Voltage	V_{RWM}	$I_R \leq 1\mu A$			2.5	V
Reverse Leakage Current	I_R	V_{RWM} = 2.5V		0.1	0.5	µA
Snap Back Voltage	V_{SB}	I_{SB} = 50mA	2.0			V
Clamp Voltage	V_C	I_{PP} = 1A, t_p = 8/20µs, Any I/O to Ground		4.5		V
		I_{PP} = 10A, t_p = 8/20µs, Any I/O to Ground		7.5		
		I_{PP} = 25A, t_p = 8/20µs, Any I/O to Ground		12		
		I_{PP} = 45A, t_p = 8/20µs, Line-to-Line[1], two I/O Pins connected together on each line		19		
Dynamic Resistance[2]	R_{DYN}	TLP, t_p=100ns, Any I/O to Ground		0.1		Ω
ESD Withstand Voltage	V_{ESD}	IEC 61000-4-2 (Contact)	±30			kV
		IEC 61000-4-2 (Air)	±30			kV
Diode Capacitance	$C_{I/O\ to\ GND}$	Between I/O Pins and Ground V_R = 0V, f = 1MHz		2.5		pF
	$C_{I/O\ to\ I/O}$	Between I/O Pins V_R = 0V, f = 1MHz		1.2		pF

Notes:
1. Rating with 2 pins connected together per sugguested diagram (For example, pin1 is connected to pin 10, pin 2 is connected to Pin 9, Pin 4 is connected to pin 7 and pin 5 is connected to pin 6)
2. Transmission Line Pulse (TLP) with 100ns width, 2ns rise time, and average window t1=70ns to t2= 90ns

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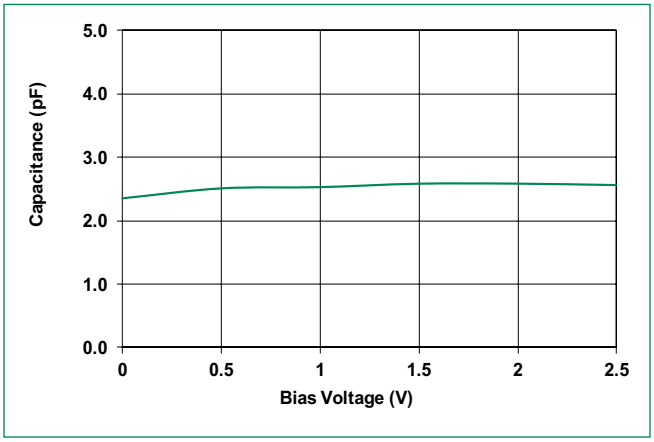
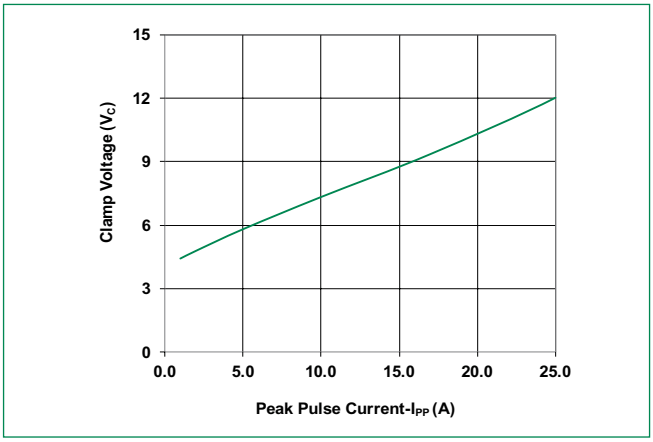
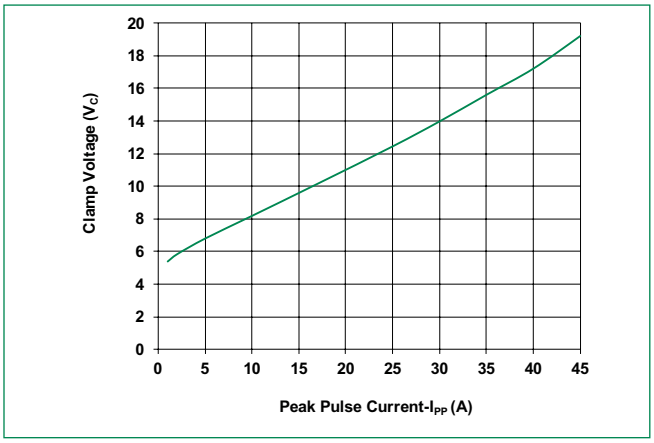
Capacitance vs. Reverse Bias



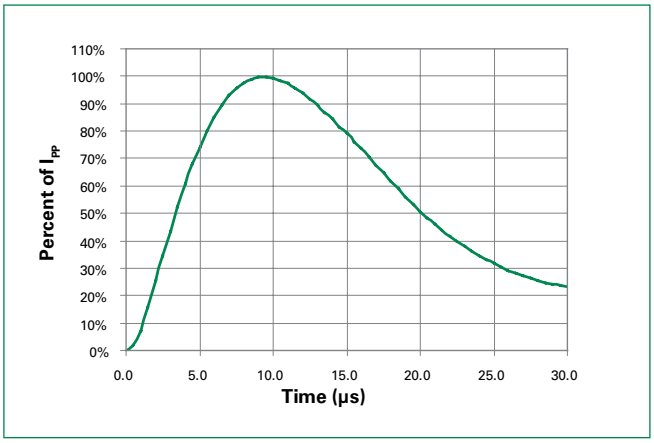
Clamping Voltage vs. I_{PP} (I/O to GND)



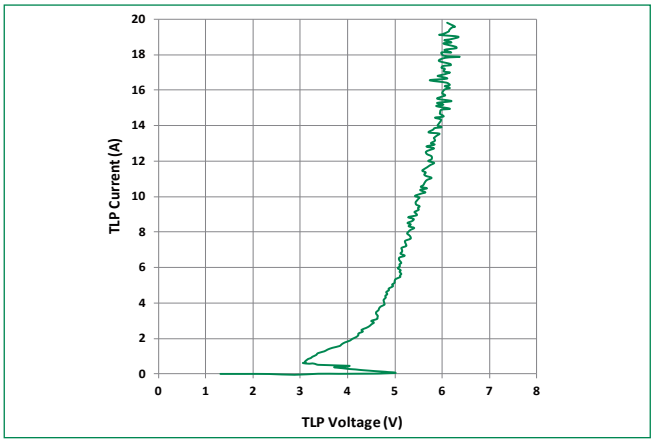
Clamping Voltage vs. I_{PP} (Line-to-Line)



8/20µS Pulse Waveform



Transmission Line Pulsing(TLP) Plot



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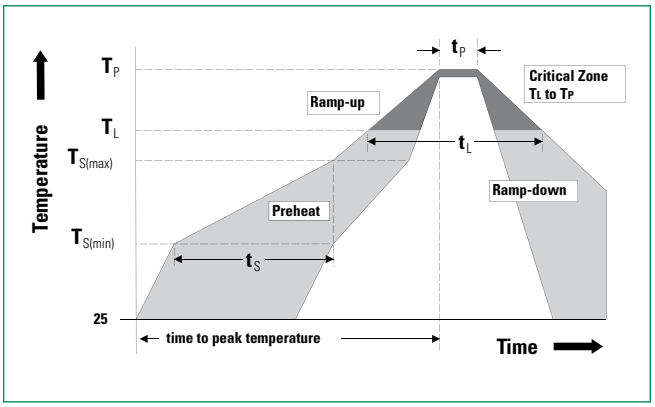
Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	**- Temperature Min ($T_{s(min)}$)**	150°C
	- Temperature Max ($T_{s(max)}$)	200°C
	- Time (min to max) (t_s)	60 – 120 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		3°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/second max
Reflow	**- Temperature (T_L) (Liquidus)**	217°C
	- Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_p)		$260^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		30 seconds
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature (T_p)		8 minutes Max.
Do not exceed		260°C



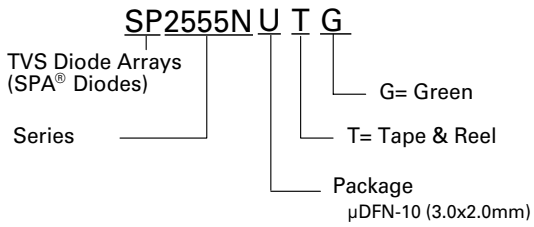
Ordering Information

Part Number	Package	Marking	Min. Order Qty.
SP2555NUTG	µDFN-10 (3.0x2.0mm)	SP2555	3000

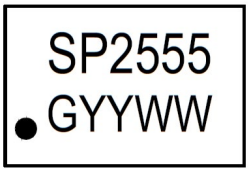
Product Characteristics

Lead Plating	PPF
Lead Material	Copper Alloy
Substrate Material	Silicon
Body Material	Molded Compound
Flammability	UL Recognized compound meeting flammability rating V-0

Part Numbering System



Part Marking System



First row= Part Name= SP2555
Second row= Assembly Code+ Date Code

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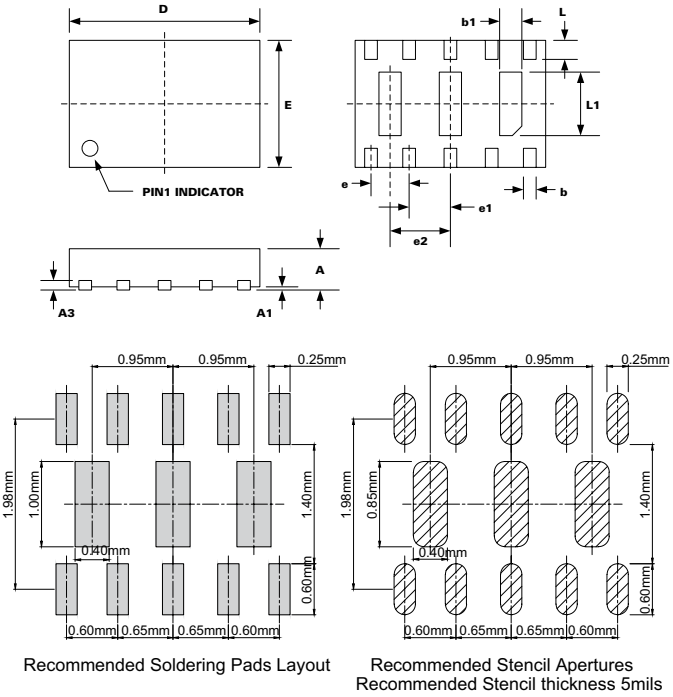
Package Dimensions — µDFN-10 (3.0x2.0mm)



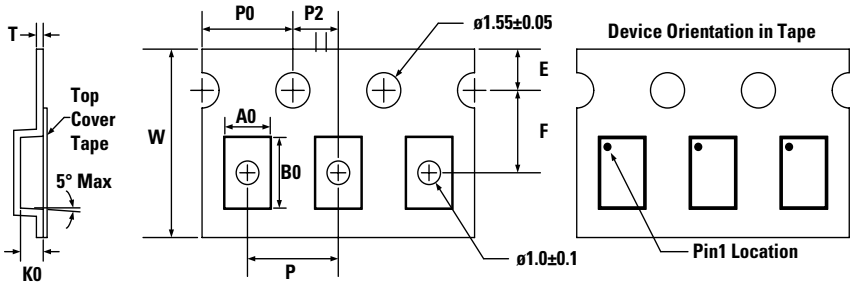
Recommended Soldering Pads Layout

Recommended Stencil Apertures
Recommended Stencil thickness 5mils

Package	µDFN-10 (3.0x2.0mm)					
JEDEC	MO-229					
Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	0.50	0.60	0.65	0.020	0.024	0.026
A1	0.00	0.03	0.05	0.000	0.001	0.002
A3		0.15 Ref			0.006 Ref	
b	0.15	0.20	0.25	0.006	0.008	0.010
b1	0.25	0.35	0.45	0.010	0.014	0.018
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.90	2.00	2.10	0.075	0.079	0.083
e		0.60 BSC			0.024 BSC	
e1		0.65 BSC			0.026 BSC	
e2		0.95 BSC			0.037	
L	0.25	0.30	0.35	0.010	0.012	0.014
L1	0.95	1.00	1.05	0.037	0.039	0.041

Notes :
1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
5. Package surface matte finish VDI 11-13.

Tape & Reel Specification — µDFN-10 (3.0x2.0mm)



Package	µDFN-10 (3.0x2.0mm)
Symbol	Millimeters
A0	2.30 +/- 0.10
B0	3.20 +/- 0.10
E	1.75 +/- 0.10
F	3.50 +/- 0.05
K0	1.0 +/- 0.10
P	4.00 +/- 0.10
P0	4.00 +/- 0.10
P2	2.00 +/- 0.10
T	0.3 +/- 0.05
W	8.00 +0.30/- 0.10

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