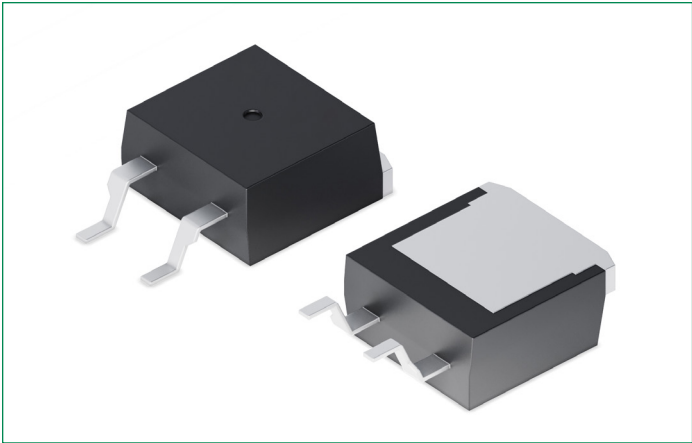


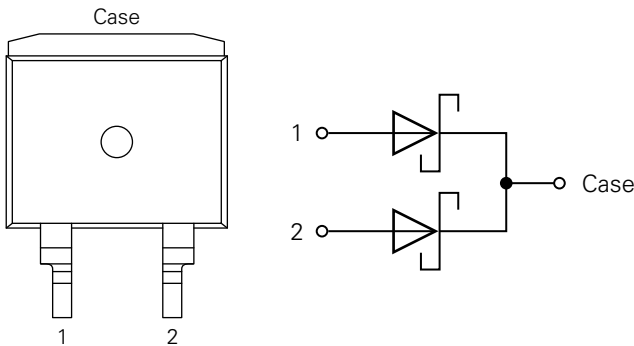
LSIC2SD065D40CC

650 V, 2× 20 A SiC Schottky Barrier Diode

RoHS



Pinout Diagram (TO-263-2L)



Features

- Positive temperature coefficient
- 175 °C maximum operating junction temperature
- Excellent surge current capability
- Extremely short switching time, temperature-independent switching behavior
- Reduced switching losses compared to Si bipolar diodes
- MSL 1 rated

Applications

- Boost diodes in PFC or DC/DC stages
- Switch mode power supplies
- Solar inverters
- Uninterruptable power supply
- Battery chargers
- High speed rectification

Product Summary

Characteristic	Value	Unit
V_{RRM}	650	V
I_F ($T_C \leq 135\text{ °C}$)	22	A
Q_C ($V_R : 0-400\text{ V}$)	63	nC

* I_F and Q_C shown is the per leg rating

Maximum Ratings

Symbol	Characteristics	Conditions	Value	Units
V_{RRM}	Repetitive peak reverse voltage	–	650	V
V_R	DC blocking voltage	–	650	V
I_F	Continuous forward current (per leg/per component)	$T_c = 25\text{ }^{\circ}\text{C}$	48 / 96	A
		$T_c = 135\text{ }^{\circ}\text{C}$	22 / 44	
		$T_c = 140\text{ }^{\circ}\text{C}$	20 / 40	
I_{FSM}	Non-repetitive forward surge current (per leg)	$T_c = 25\text{ }^{\circ}\text{C}$, $t_p = 10\text{ ms}$, Half sine pulse	95	A
$\int I^2 dt$	$I^2 t$ (per leg)	$T_c = 25\text{ }^{\circ}\text{C}$, $t_p = 10\text{ ms}$, Half sine pulse	45	A ² s
P_{Tot}	Power dissipation (per leg/per component)	$T_c = 25\text{ }^{\circ}\text{C}$	150 / 300	W
		$T_c = 110\text{ }^{\circ}\text{C}$	65 / 130	
T_{vj}	Virtual junction temperature range	–	–55 to +175	$^{\circ}\text{C}$
T_{stg}	Storage temperature range	–	–55 to +175	$^{\circ}\text{C}$
T_{sld}	Soldering temperature	Plastic body for 10 s	260	$^{\circ}\text{C}$

Thermal Characteristic

Symbol	Characteristic	Value	Unit
$R_{th(j-c)} \text{ MAX}$	Thermal Resistance, junction-to-case (per leg/per component)	1.0 / 0.5	K/W

Electrical Characteristics

Symbol	Characteristic	Conditions	Value			Unit
			Min.	Typ.	Max.	
V_F	Forward voltage	$I_F = 20\text{ A}$, $T_{vj} = 25\text{ }^{\circ}\text{C}$	–	1.5	1.8	V
		$I_F = 20\text{ A}$, $T_{vj} = 175\text{ }^{\circ}\text{C}$	–	1.7	–	
I_R	Reverse current	$V_R = 650\text{ V}$, $T_{vj} = 25\text{ }^{\circ}\text{C}$	–	3	100	μA
		$V_R = 650\text{ V}$, $T_{vj} = 175\text{ }^{\circ}\text{C}$	–	70	–	
C	Total capacitance	$V_R = 1\text{ V}$, $f = 1\text{ MHz}$	–	842	–	pF
		$V_R = 200\text{ V}$, $f = 1\text{ MHz}$	–	105	–	
		$V_R = 400\text{ V}$, $f = 1\text{ MHz}$	–	91	–	
Q_C	Total capacitive charge	$V_R = 400\text{ V}$, $Q_C = \int C(V) dV$	–	63	–	nC
E_C	Capacitance stored energy	$V_R = 400\text{ V}$	–	6.9	–	μJ

Note: All ratings are per leg unless otherwise specified; $T_{vj} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Characteristic Curves

Figure 1. Typical Forward Characteristics (per leg)

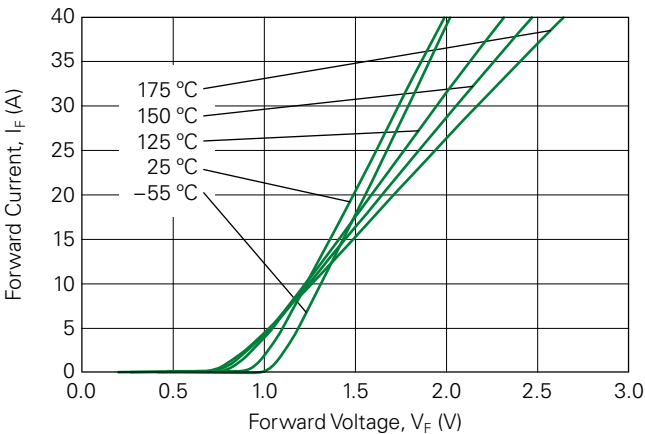


Fig. 2. Typical Reverse Characteristics (per leg)

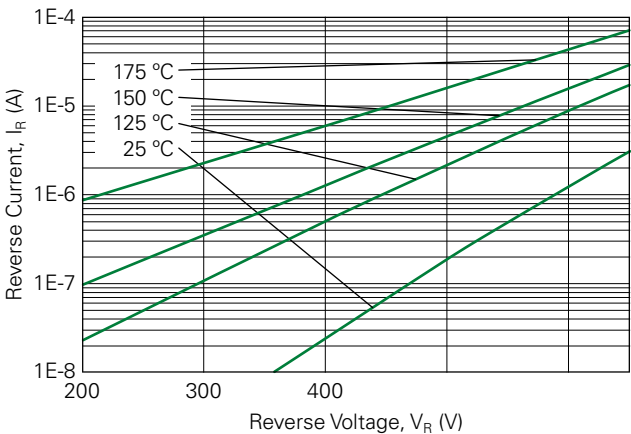


Fig. 3. Power Derating (per leg)

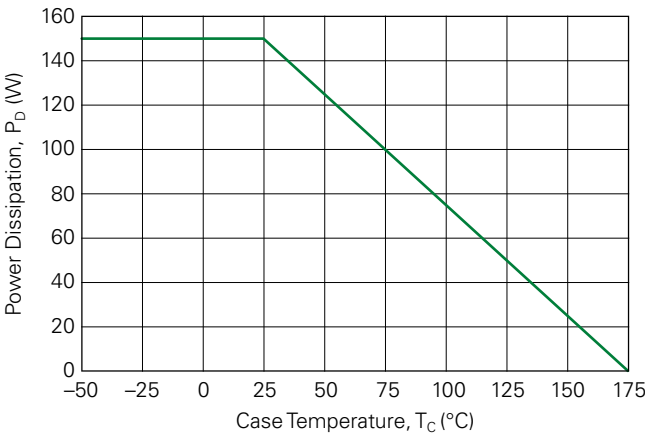


Fig. 4. Current Derating (per leg)

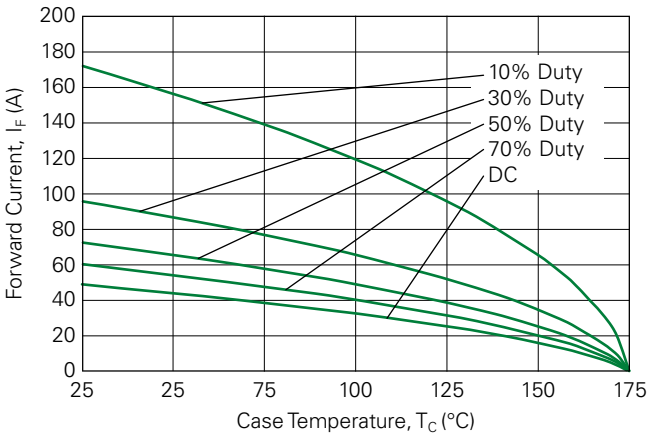


Figure 5. Capacitance vs. Reverse Voltage (per leg)

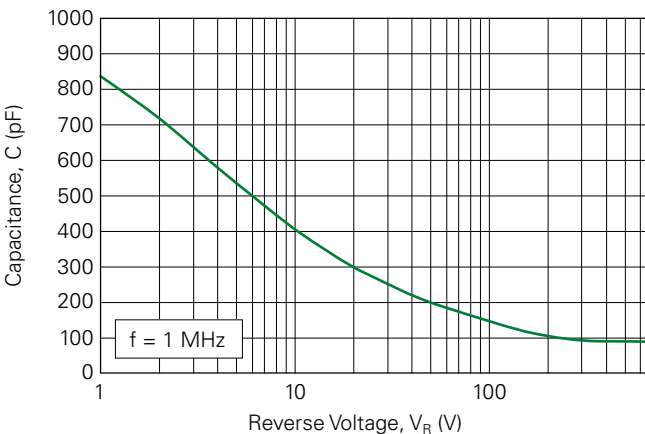


Fig. 6. Capacitive Charge vs. Reverse Voltage (per leg)

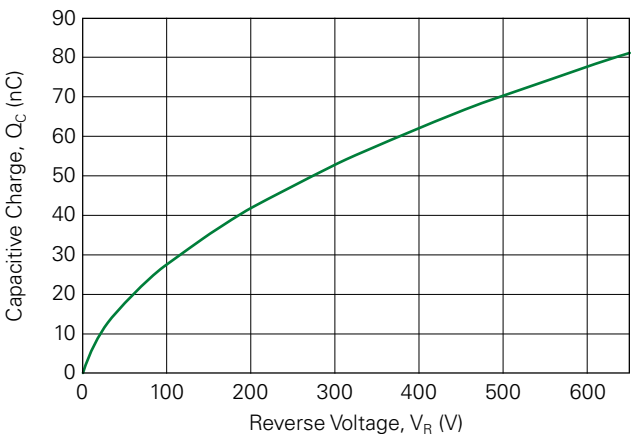


Fig. 7. Stored Energy vs. Reverse Voltage (per leg)

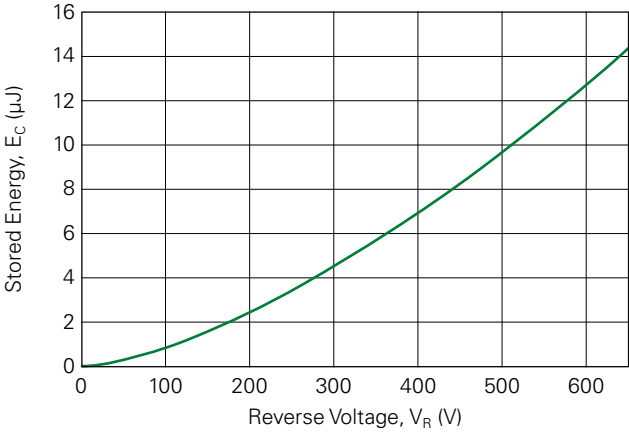
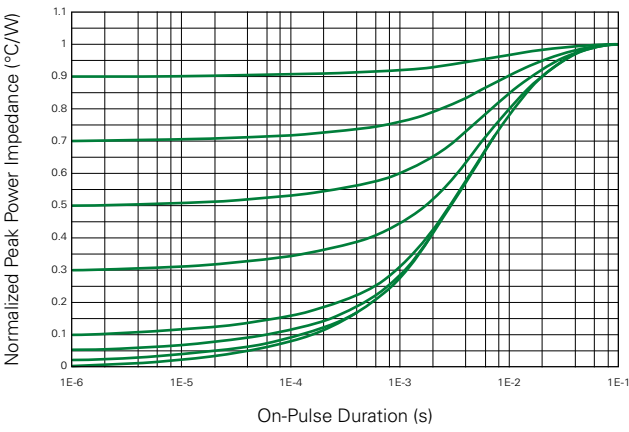
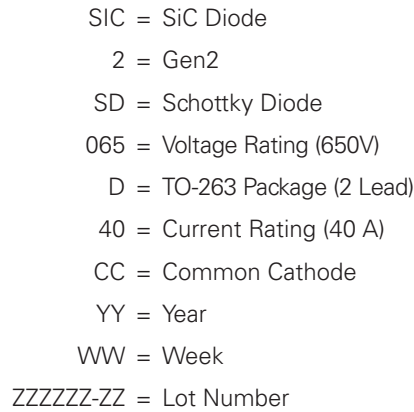


Fig. 8. Transient Thermal Impedance (per leg)



Ordering Information

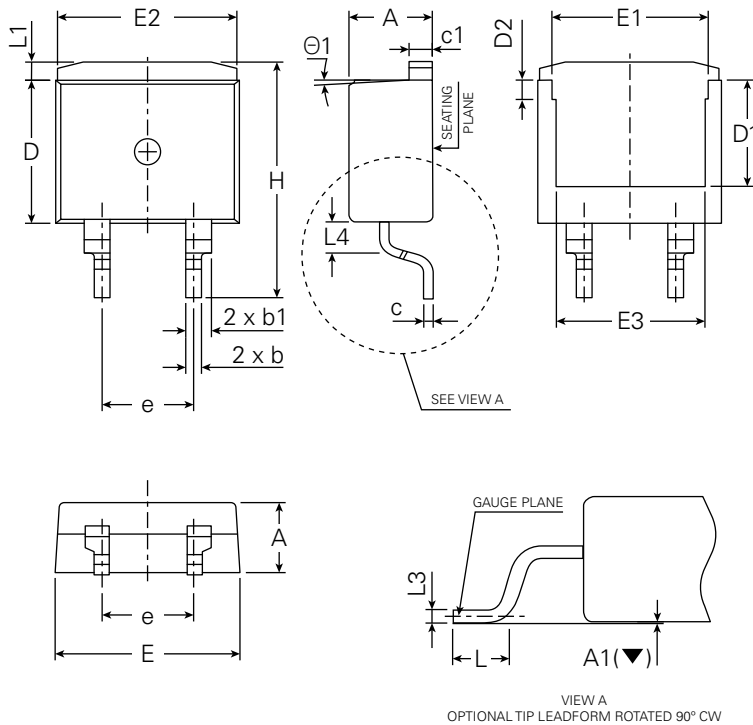


Part Number	Marking	Packing Mode	M.O.Q
LSIC2SD065D40CC	LSIC2SD065D40CC	Tape and Reel	–

[illegible]

1. MATERIAL: PS (Poly Stylene)
2. ESD (Electrostatic Discharge) CONTROL: LESS THAN ± 100 [Volts]
3. SURFACE RESISTANCE: LESS THAN $10^7[\Omega/\text{cm}^2]$
4. Unit: Millimeter (mm)

Part Outline Drawing (TO-263-2L)

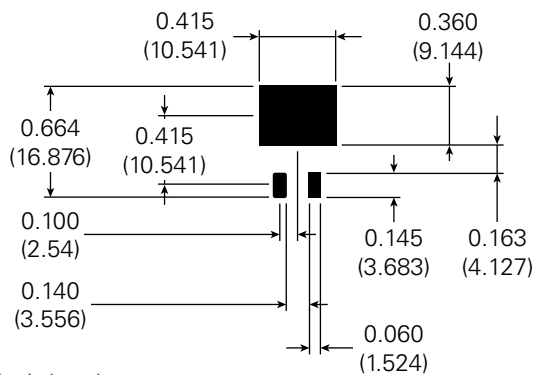


Notes:

1. These dimensions do not include protrusions of the mold.
2. The "()" mark is the reference.
3. Coplanarity: Max 0.10 mm.
4. Metal finish – matte pure tin plating except trim area.
5. All plastic surfaces are polish finish
6. Nominal 0.25 radius on all body edges and corners.

Symbol	Inches			Millimeters		
	Min.	Typical	Max.	Min.	Typical	Max
A	0.169	0.181	0.185	4.30	4.60	4.70
A1(▼)	0.000	–	0.008	0.00	–	0.20
b	0.028	0.031	0.035	0.70	0.80	0.90
b1	0.046	0.050	0.054	1.18	1.28	1.38
c	0.018	0.020	0.024	0.45	0.50	0.60
c1	0.049	0.051	0.055	1.25	1.30	1.40
D	0.354	0.362	0.370	9.00	9.20	9.40
D1	0.264	0.272	0.280	6.70	6.90	7.10
D2	0.043	0.051	0.059	1.10	1.30	1.50
E	0.386	0.394	0.402	9.80	10.00	10.20
E1	0.323	0.331	0.339	8.20	8.40	8.60
E2	0.382	0.390	0.398	9.70	9.90	10.10
E3	0.307	0.315	0.323	7.80	8.00	8.20
e	0.20 BSC			5.08 BSC		
H	0.591	0.602	0.614	15.00	15.30	15.60
L	0.079	0.091	0.102	2.00	2.30	2.60
L1	0.039	0.047	0.055	1.00	1.20	1.40
L3	0.010 BSC			0.254 BSC		
L4	(0.079)			(2.00)		
Θ1	(3°)			(3°)		

Recommended Solder Pad Layout



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Part of:

