Paralleling and Series-Connecting of Power Semiconductors

Objectives

Voltage and current put physical limits on every individual power semiconductor. Once one of these limits is reached, larger devices can be used if available. Alternatively, power semiconductors can be paralleled to increase the current carrying capability or get series-connected to increase blocking voltages. This document suggests features to be considered in both cases.

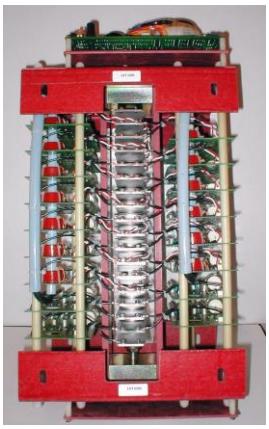

Figure 1: Stack of 13 GTOs in series to support switching 20 kV

Applications

- Thyristor-based high-power applications
- High-current low-voltage MOSFET-drives
- Medium-voltage drives
- Pulse-power applications

Target Audience

This document is intended for all developers serving applications that cannot easily be constructed using single power devices and therefore need to consider paralleling or series-connecting of power semiconductors.

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Introduction

Power semiconductors have seen a remarkable development in the last decades and by today, devices with blocking voltages in the regime of several kilovolts are available. Similarly, single switches to handle kiloamps of current became state of the art.
Despite these impressive numbers, there are use-cases that cannot be served using a simple approach based on a single device. Material handling in forklifts is such an application. With the urge to keep the drive-train's voltage at 48 V while achieving tens of kilowatt in power, currents grow to hundreds of amps. The preferred switch is a low-voltage MOSFET, but as there is no single device to carry the current, paralleling becomes necessary.

In higher voltage classes, medium-voltage converters are designed with individual stages that can block 2-3 kV. Though IGBTs with such high blocking voltages are available, it can be a more economical solution to replace single switches with series-connected devices with lower blocking voltages.

Finally, in high-voltage DC-transmission (HVDC), DC-voltages up to 1000 kV recently were installed. Here too, series-connection of thyristors is one option to cope with such high voltage levels.
Because of their dedicated technological features, it is rather simple to parallel IGBTs or MOSFETs, while a series-connection of these components tends to be challenging. With thyristors, GTOs, and bipolar diodes, it is just the opposite way. Series-connecting is the simpler task while paralleling those devices comes with certain challenges.

1. Paralleling IGBTs and MOSFETs

It is mandatory to only consider devices for paralleling which are of the same kind and come from the same manufacturer to create a reliable working system. If the effort can be done, selecting devices with matched forward voltages is beneficial.
Modern IGBTs and MOSFETs have an output characteristic that features a positive temperature coefficient regarding the temperature dependance of the forward voltage. As seen in Figure 2, the forward voltage for the same current increases at higher temperature.

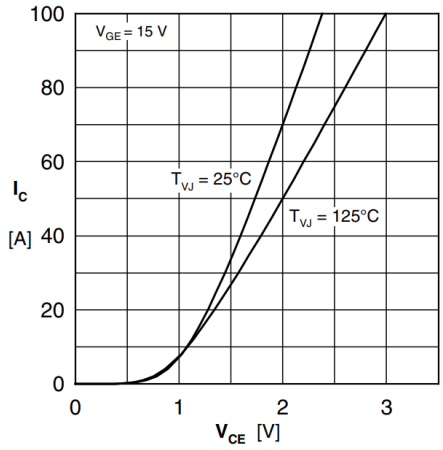

Figure 2: Output characteristic for an IGBT, example taken from the IXA60IF1200NA

When paralleling devices, this is a wanted feature as it leads to an active balancing and equal sharing of continuous current. In case an initial imbalance occurs, the chip with the lowest temperature takes the highest current and thus heats up. As this increases its forward voltage compared to the paralleled devices, another "cold" chip will then take over more current quickly until the forward voltage of all devices reaches the same value. Within the inherent device tolerances, this finally leads to an equal current sharing. These tolerances can be reduced further by testing and selecting devices with matched V_{CE}-values.
While this is valid for continuous current flow, the challenge in paralleling devices lies within the dynamic processes, designing an optimized layout to achieve electrical symmetry, and properly build gate-driver circuitry.

1.1. Details in Dynamic Processes

When paralleling devices, care needs to be taken to achieve the same impedance for all paralleled paths. This particularly includes parasitic resistances and inductances.
Every trace of copper, each terminal, connection, or wire adds stray inductance to the schematic. A detailed view on a generic device including the stray inductances is drawn in Figure 3.

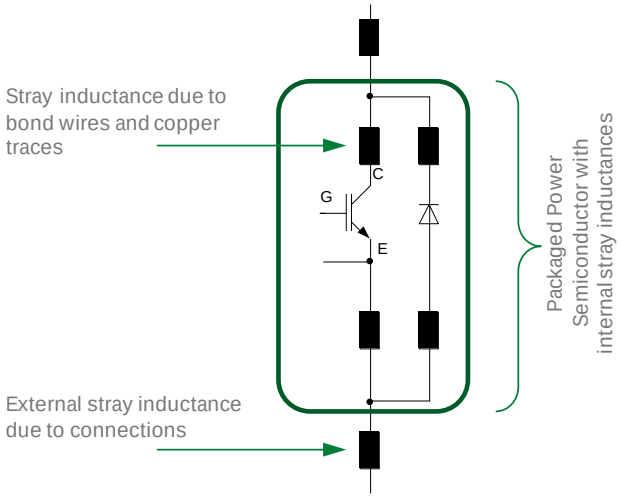

Figure 3: Schematic of a power semiconductor setup including stray inductances

For physical reasons, the internal stray inductances cannot be eliminated. With proper design, these parasitic elements can be reduced to just a few nanohenry and feature very narrow tolerances between devices of the same kind. For paralleling devices, paying attention to the external stray inductance is important. Different inductances for paralleled devices can lead to a multitude of detrimental effects including the instantaneous current sharing, the resulting switching losses, and even potential damage to the devices.
The root causes for this issue can be explained by looking at Figure 4. Here, two devices are paralleled by simply connecting all terminals. For several reasons, this is not a recommended version.

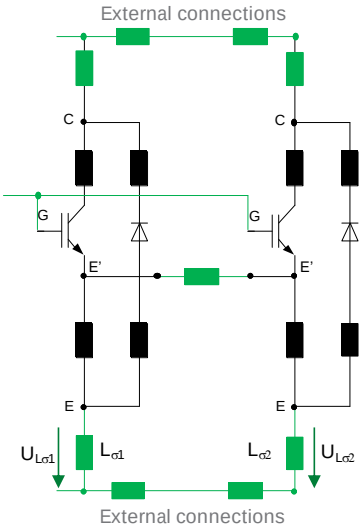

Figure 4: Paralleling IGBTs using external connections

In case the inductances $L_{\sigma 1}$ and $L_{\sigma 2}$ differ from each other, at least three different effects can occur:

- As the devices are operated at the same voltage UDC, the current change rate di/dt = UDC/Ls is different. This leads to differences in the time it takes to turn a given current on or off. An imbalance in instantaneous current sharing is the unwanted result.
- With unequal current change rates, switching losses in the slower device tend to be higher which leads to higher temperatures for the same current. In turn, other devices must carry larger currents, fostering an imbalance in steady-state operation.
- The voltage induced during switching is different as well. This leads to driving voltage being present in a path with very low loop resistance. Assuming the difference is just a few millivolts, but the loop's resistance is in the milliohm regime, the resulting circulating current can grow to tens of amps. The weakest link is the single bond-wire connected to the auxiliary emitter E'. Too high circulating current can fuse that bond wire. Controlling the corresponding switch would then require the gate-current to flow through the main emitter which leads to higher switching losses and potentially oscillations.

1.2. Electrical Symmetry

With respect to Figure 4, and looking at where current enters and exits the setup, different options become available, as displayed in Figure 5.

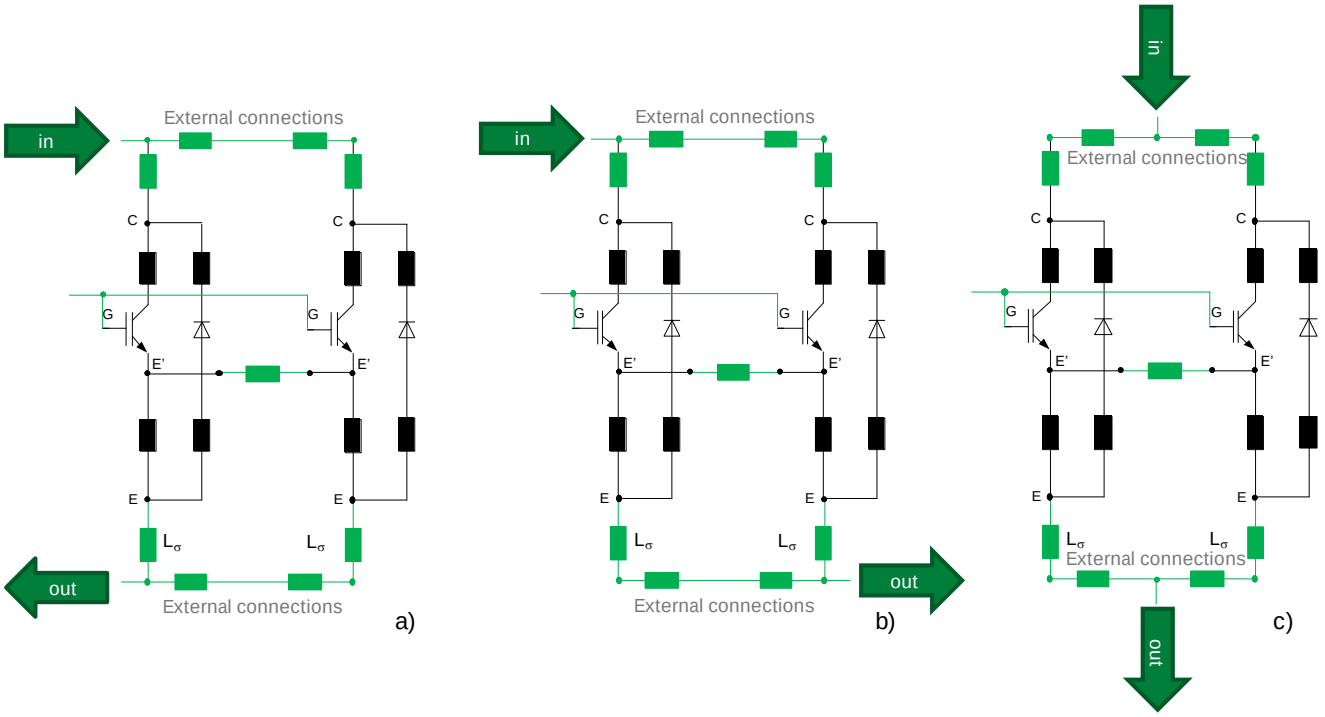

Figure 5: Detailed look at the position to connect to the paralleled devices

For the two paralleled devices in Figure 5 a), the paths for the current to flow through differ a lot which leads to unbalances. In parts 5 b) and 5 c), the number of elements the current has to pass is identic and thus a well-balanced situation arises. These two pictures also reveal that electrical symmetry may differ from optical symmetry. The preferred solution remains the one in 5 c).

The information from the schematic in Figure 5 can be transferred to a corresponding layout. Figure 6 is a sketch to represent the real-world appearance and the influence of properly choosing the point of connection.

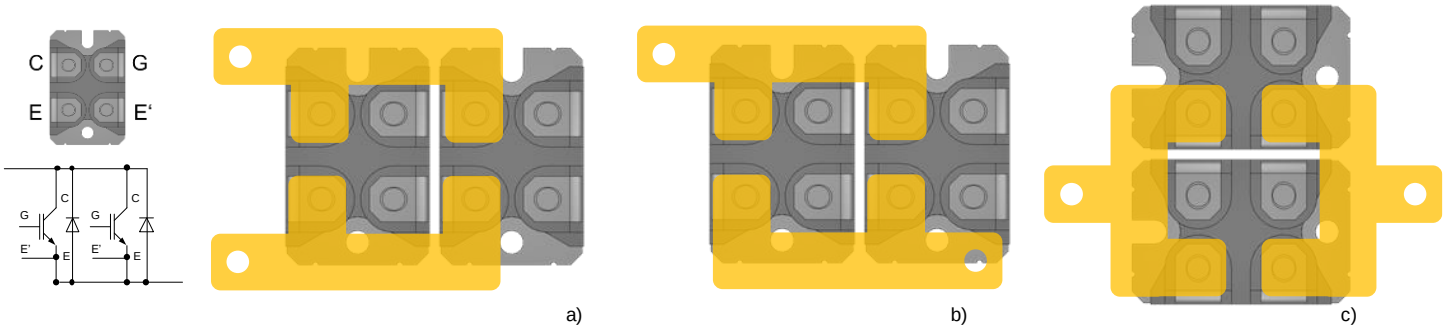

Figure 6: Paralleling two miniBLOCs, SOT-227b

The connection depicted could be created from PCB or metal bars. Depending on the topology to be built, the stray inductance inherently included might be disturbing. In such cases, building low-inductive designs using laminated structures leads to better results. A basic example on how to set up a low-inductive DC-link for a half-bridge is drawn in Figure 7.

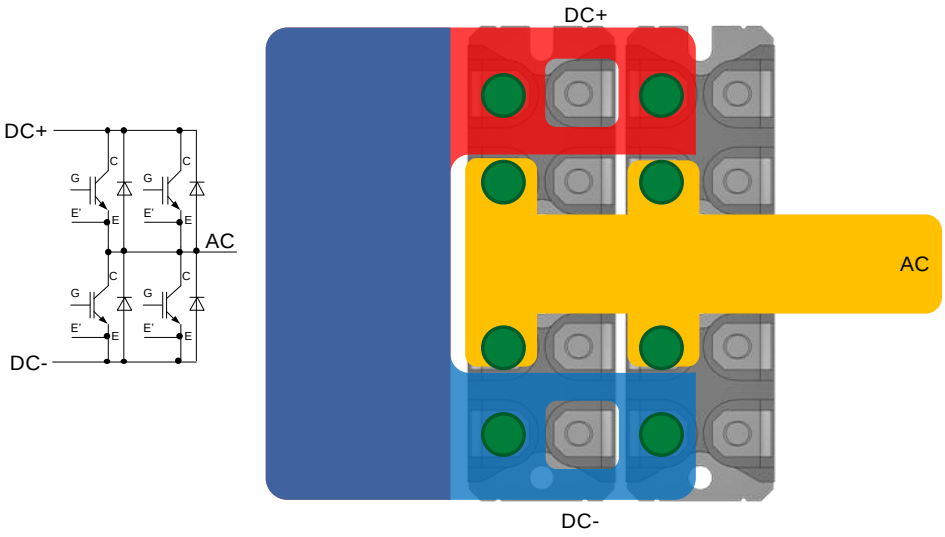

Figure 7: Half-bridge constructed from paralleled miniBLOC devices

The laminated structure should overlap as much as possible to increase the parasitic capacitance. The cut-away in the center is only introduced for simplification and better overview.

1.3. Gate-drive Consideration for Paralleling

When paralleling IGBTs or MOSFETs, precisely synchronized gate-signals are of utmost importance. Ideally, all switches turn on and off in the same instant. Due to the inherent device tolerances, perfect synchronization may not be achieved and minor deviations in the tens of nanoseconds remain. This is considered acceptable, though it is highly recommended to verify that the thermal and electrical behavior of the final setup is closely examined.

Looking at control schemes to drive paralleled devices, driving all of them with the same gate signal is an option. As explained in Figure 4, a too simple approach may lead to loops with very low impedances and to potential trouble with circulating currents. A countermeasure to improve the situation is splitting the gate-resistors into one gate- and one emitter-resistor. The correlating scheme is given in Figure 8.

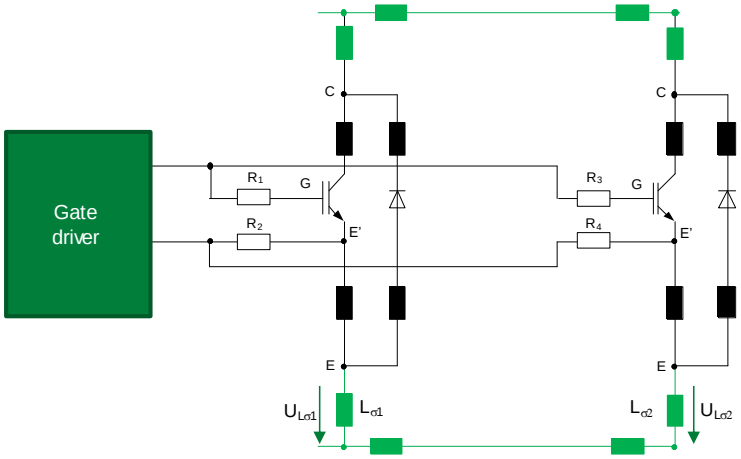

Figure 8: Eliminating low-resistant loops

It is good practice to have a single gate resistor R_g replaced by the combination of $R_{1/3}=1/3 \cdot R_g$ and $R_{2/4}=2/3 \cdot R_g$. The loop that now forms includes two emitter-resistances in series, usually adding up to several Ohm at least. A voltage difference across the inductors of a few millivolts thus can only drive a circulating current of a few milliamps.

At very high power levels, when a single gate-driver IC or gate-driver core cannot provide the necessary gate-current summed up from all devices, two further options can be considered:

- Use a central gate driver connected to the control side and add individual booster stages to drive each individual power semiconductor. This is often done when paralleling IGBTs in high-power packages like disc devices to achieve currents exceeding 2 kA.
- Install an individual gate driver for each power semiconductor. This solution is mainly looked at when it comes to driving IGBTs with blocking voltages 3.3 kV and above, each capable of handling hundreds of amps and paralleling leads to larger geometric arrangements.

The first solution keeps the timing differences between the individual gate-signals very low and shifts the thermal challenges from the central gate driver to the booster stages, thus simplifying thermal management. Therefore, it is the preferred way to proceed.

If individual gate-drivers are considered, precise timing despite tolerances needs to be achieved. It is good practice to align all gate-signals, measured directly at the device, within a window of ≤100 ns.

The situation may also be handled by paralleling inverters instead of paralleling devices. In that case, synchronizing the different systems by a superordinated control becomes the task. Here too, equal load-sharing needs to be achieved.

2. Series Connection of IGBTs

Though rarely seen, the series-connection of IGBTs or MOSFETs is a technical option to increase the blocking voltage. Especially in medium-voltage drives, this approach coexists and compliments multilevel topologies to serve applications that require output voltages in the medium-voltage regime beyond 1500 V_{AC}.

Figure 9 is the schematic of a classical 2-level medium-voltage inverter setup.

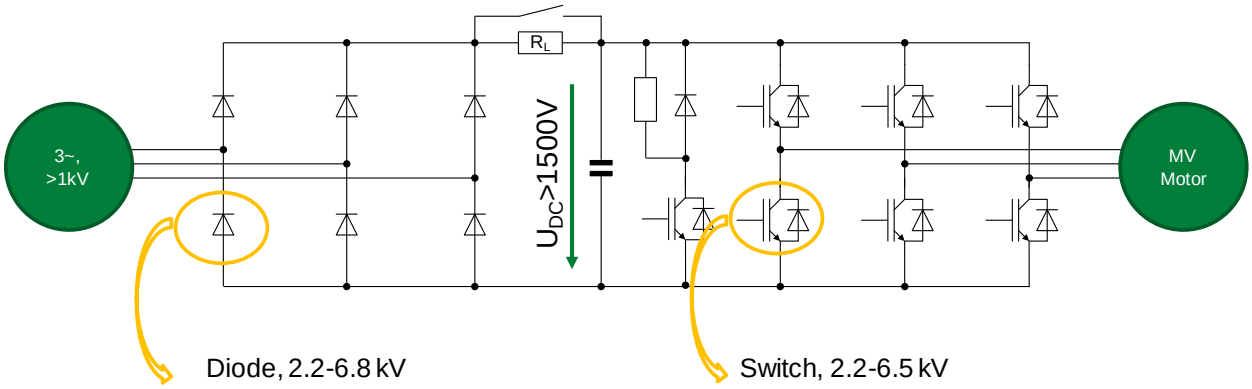

Figure 9: 2-Level inverter for medium-voltage drives applications

From today's portfolio, power semiconductors with blocking voltages up to 6.5 kV can be chosen, which allows for DC-link voltages of up to 4500 V.
Once these levels are no longer sufficient, either series-connection of devices or a change to multilevel topologies can be considered. While series-connecting of isolated devices like high-power IGBT-modules leads to challenges with the isolation strength, disc-style devices like Littelfuse Press-pack IGBTs can be stacked and series-connected without these isolation issues. The challenge remains the control of such a switch. In series-connection, the devices no longer share a common emitter potential and thus it is mandatory to use individual gate-drivers. Though IGBTs can temporarily tolerate a high current, they rather quickly get destroyed by overvoltages. Synchronizing the switching in series-connected devices therefore becomes a critical issue to prevent the semiconductors from being damaged.

In the overview given in Figure 10 it becomes obvious that even identical gate drivers feature delays and more importantly delay deviations between two parts. Including the necessary galvanic insulation, it is important to get the gate-signals meticulously aligned. A timing window of 50 ns or below has proven to work properly.

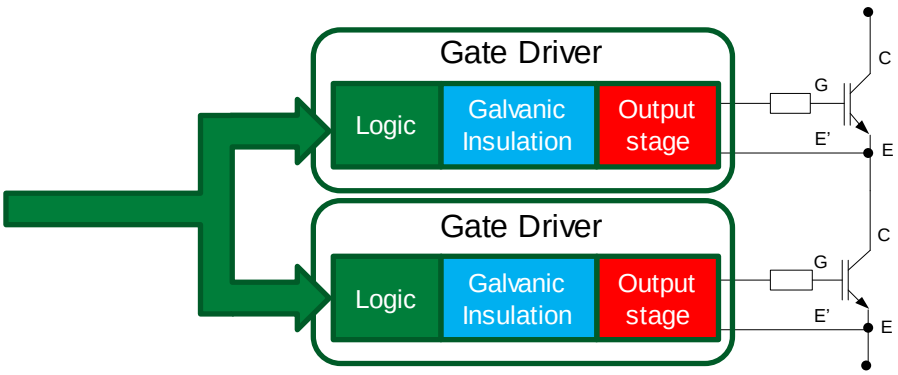

Figure 10: Gate-drive setup in series-connected switches

Such values can best – or only – be reached with selected, matched semiconductors that feature highly similar parameters regarding gate-charge and turn-on/turn-off times and -delays. For high-power Press-pack IGBTs it is also recommended to add selected and matched freewheeling diodes with similar values for recovery charge Q_{rr} and reverse recovery current I_{rr}.

3. Series Connection of Thyristor-style Devices

Thyristor-style devices include not only the classical diodes and thyristors, but also their relatives Gate-Turn-Off thyristor (GTO), MOS-Controlled Thyristor (MCT), and the Insulated Gate Controlled Thyristor (IGCT). These devices are typically stacked in applications like high voltage DC-transmission (HVDC) or in medium-voltage rectifiers.

Here too, it is recommended to group selected devices that feature similar values in recovery charge Q_{rr} and reverse recovery current I_{rr}.

As discussed earlier, device blocking voltage ratings of up to 6.5 kV are commercially available, with devices reaching or even exceeding 8.5 kV in development. To this end, the application requires devices to be connected in series. The problems associated with operation arise largely from the inevitable, minor variations in the device characteristics. There are two areas that must be addressed when considering series operation: static voltage balancing and dynamic voltage balancing.

Static voltage balancing

In Figure 11, the blocking characteristics for three devices T_1, T_2 and T_3 that are considered identical is compared in detail. When connected in series, all devices must carry the same leakage current and, as a result, the voltage will be distributed as denoted by v_1, v_2 and v_3.

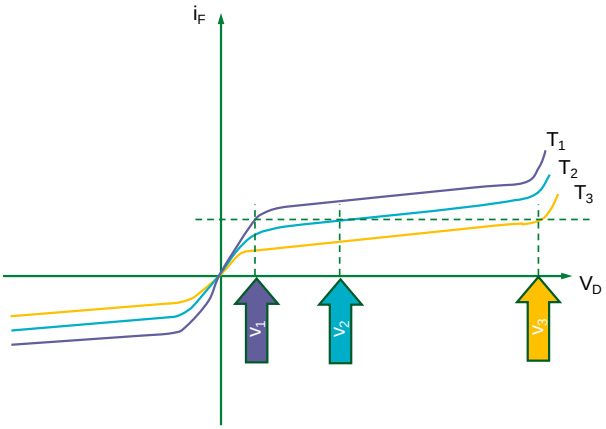

Figure 11: Variations in off-state characteristics

This would either lead to an over voltage condition and device failure or necessitate impractical levels of voltage de-rating. There are several practical solutions to this problem, the most common one being the use of voltage sharing resistors connected in parallel with each device. If the resistor current is significantly greater than the device leakage current, then the voltage balancing becomes independent of the individual semiconductor device's characteristics. Worst case conditions are present when connecting *n* devices with *n-1* high leakage devices and one low leakage device. In this case, the parallel sharing resistor for each device is approximated by Equation 1

$$R = \frac{n \cdot V_D - V_S}{(n-1)(I_{kx} - I_{kn})} \quad (1)$$

In this equation, V_D is the desired voltage across any device, V_S is the supply voltage the series-connection is connected to while I_{kx} and I_{kn} represent the maximum and minimum device leakage current respectively.

This can often lead to high power dissipation in the parallel resistors, sometimes in the order of kilowatts. To make a more efficient solution, it is common to match the device characteristics. Further gains are possible by taking maximum device junction temperature and working voltage into account as opposed to device rating. In many applications, it is possible to reduce power dissipation in these resistors to less than 10 W per device.

Dynamic voltage balancing

There are several aspects to consider under dynamic voltage balancing, including turn-on, turn-off, static dv/dt, and reverse recovery where applicable.

Production variations in switching delays can be as much as 500 ns under normal operating conditions. Under these circumstances, the last device to turn-on and the first device to turn-off would have to support the entire supply voltage – inevitably leading to device failure. By using very strong gate drive pulses, the delay time for a given device, and moreover the effect of production variations, can be minimized as presented in Figure 12, to typically <50 ns. In applications where symmetric devices undergo dynamic reverse biasing, there is a requirement to balance the variations of recovery charge; this normally dominates the design criteria. As with static voltage balancing, there are several solutions to the problem, but the most common approach is the use of a capacitance C_s connected across the devices, normally with a series damping resistor R_s. This circuit serves to limit dv/dt from the supply side for a given supply impedance and voltages induced by device recovery whilst also accommodating any variation in switching times. A typical, so-called snubber circuit including static balancing resistors R_p is laid out in Figure 12.

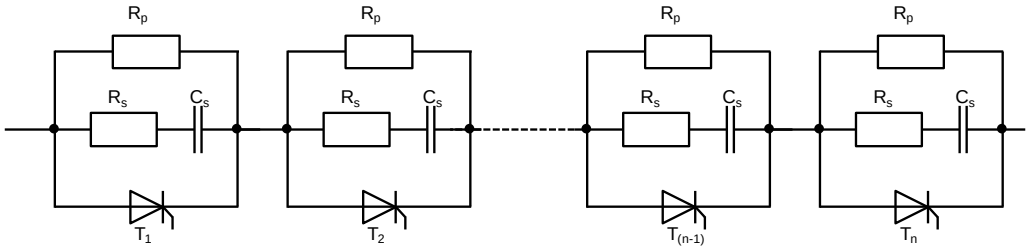

Figure 12: Typical series-connection using snubbers

The approach taken to dimension these components depends on the application to some degree, but some general guidelines are applicable, summarized in equations 2–4:

Maximum dv/dt

$$dv/dt_{(max)} = 2 \cdot \alpha \cdot \omega_n \cdot V_S = \frac{V_S \cdot R_S}{L} \quad (2)$$

Damping factor

$$\alpha = \frac{R_S}{2 \cdot \sqrt{L/C_S}} \quad (3)$$

Circuit's natural angular frequancy

$$\omega_n = 1/\sqrt{L \cdot C_S} \quad (4)$$

The inductance L in these equations represents the sum of inductances of the overall setup.

It should be noted that with *n* devices in series, the resulting resistor is $n \cdot R_s$ and the overall capacity is $n^{-1} \cdot C_s$.

In terms of balancing voltage, caused by variations in switching and recovery delays, it is common to equate the difference in delay times to charge (Δt_d). For a given Δt_d and a known switch current waveform, a value for ΔQ can be derived – the integral of the switch current waveform over the period of Δt_d. For turn-off, the same approach can be taken. For reverse recovery, where appropriate device manufacturers will supply and match devices for reverse recovery charge, Q_{rr} again results in a value ΔQ. Once known, it is then a simple matter to calculate the minimum value of snubber capacitor according to equation 5, assuming a maximum transient voltage increase of ΔV.

$$C_S = \frac{\Delta Q}{\Delta V} \quad (5)$$

The peak transient voltage can be up to 80% of the maximum device voltage rating. If the DC voltage rating were 50% of the maximum device voltage rating, then ΔV would be up to 30% of the maximum device voltage rating.

Other balancing techniques

There are some alternatives to the balancing circuits described thus far. These involve the use of avalanche devices to limit the voltage across the semiconductor, both in the static and dynamic case. Suitable avalanche devices include metal oxide varistors and avalanche diodes. This approach can be useful when it is undesirable to employ capacitive elements across the switch, for example with negative impedance loads. The application of this approach can be limited in frequency due to the power limitations of commercially available avalanche devices.

4. Paralleling of Thyristor-style Devices

In case very high currents need to be handled, paralleling devices becomes necessary.
Especially under pulsed power conditions it is not easy to guarantee that current will be shared equally between devices. This is because of variations in device delay times, device output characteristics and variations in parallel circuit impedance. Even proximity and other magnetic effects can influence current sharing in applications with very short rise times. There are numerous useful techniques that can help with these problems. Firstly, by matching parallel semiconductors by selecting devices with similar delay times and output characteristics. Furthermore, by using a strong gate pulse, it is possible to minimize the inherent current imbalance due to the semiconductor to less than 10% in most applications. To reduce the effects of circuit layout, it is important to produce symmetrical parallel current paths. For example, a single pulse forming inductor could be replaced by several inductors placed in the individual parallel circuit paths, which improves current sharing. These inductors could even be coupled.

5. Conclusion

Series-connection or paralleling of power semiconductors is a viable technique to extend the limits given by the devices currently available to the market. Care needs to be taken to include the surrounding and resulting conditions into consideration to achieve a reasonable load-sharing. If, additionally, the dedicated effects to control strategies are respected, a successful design can be found to serve even challenging applications.