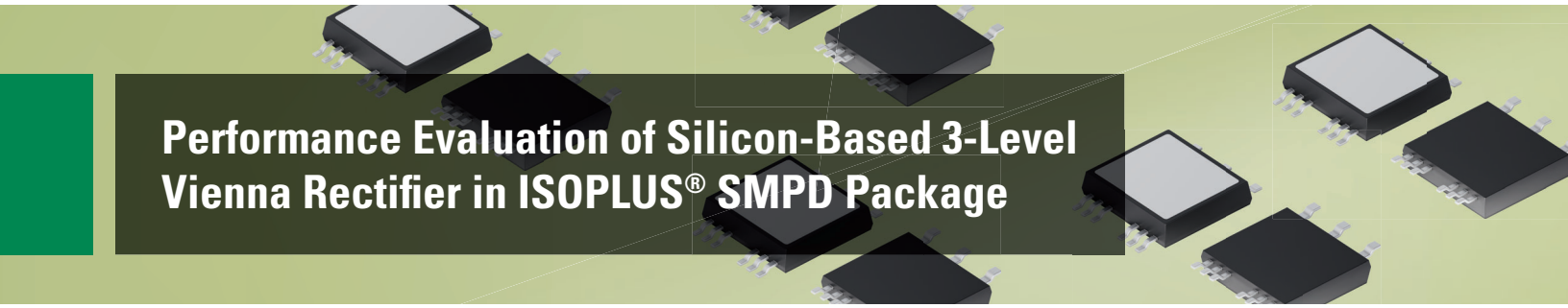

Performance Evaluation of Silicon-Based 3-Level Vienna Rectifier in ISOPLUS® SMPD Package

Abstract

Public DC-charging infrastructure is connected to the public three-phase low-voltage grid. Therefore, it must comply with international standards and the corresponding grid codes. The widely adopted Vienna rectifier makes it possible to meet this requirement and offers very high efficiency at low circuit complexity. It allows the use of fast 650 V silicon-based switches and 1200 V diodes to operate on most three-phase low voltage grid connections. In this article, measurement results are presented to convey the performance of the Vienna rectifier utilizing the compact ISOPLUS® Surface Mounted Power Device (SMPD) package, and to indicate the power- and efficiency-levels that can be achieved based on silicon technology.

Introduction

Latest developments in electric vehicle (EV) DC-chargers as of Q1/2025 show power levels up to 400 kW. These DC-chargers are normally built in a modular manner, based on power subunits with up to 100 kW output power each [1, 2]. This approach is well-known in the design of server power supplies in data centers, which comply with requirements for high efficiency, high reliability, and simple maintainability. A block diagram of such a power subunit is illustrated in Figure 1.

The power electronics inside the AC-DC subcircuit convert the line voltages into DC voltage while maintaining sinusoidal input currents, while also performing power factor correction (PFC). A common approach is to use the Vienna rectifier topology, also known as symmetric boost PFC or 3-level T-type neutral boost PFC.

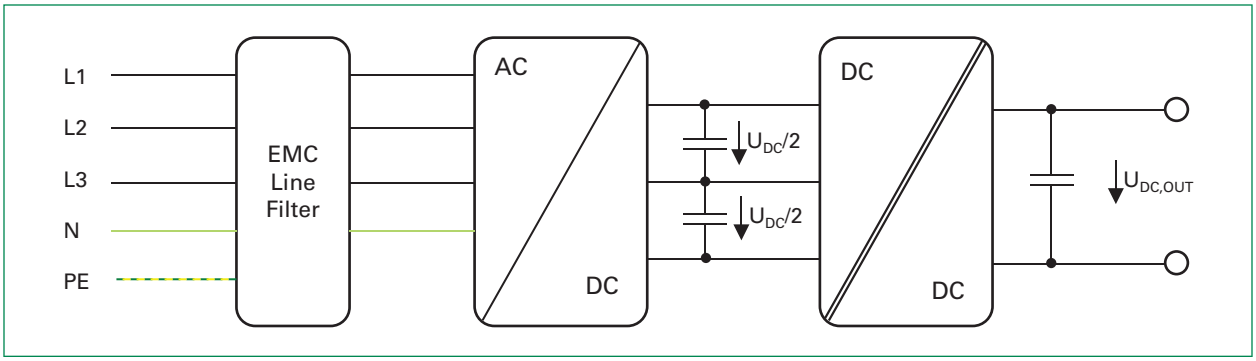

Figure 1. Block diagram of a power supply unit of a DC-charger

The 3-level Vienna Rectifier

Figure 2 depicts the circuit diagram of the Vienna rectifier. It is a three-phase boost converter, which can draw sinusoidal grid currents, correct the power factor of the line currents, and control the DC output voltage, U_{DC}. When using silicon devices such as 650 V Power MOSFETs or fast 650 V IGBTs, it can offer low-cost and low filtering efforts, but operate at high efficiency.

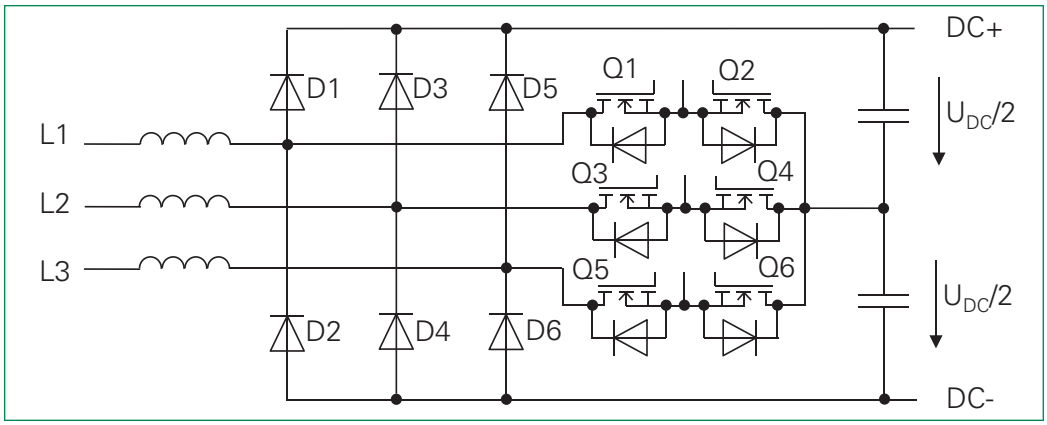

Figure 2. Circuit diagram of the 3-level Vienna rectifier

The diodes D1 to D6 need to block the DC-link voltage, U_{DC} and need to be rated for a blocking voltage of 1200 V. Thus, to achieve high switching speeds, 1200 V Si Fast Recovery Diodes (FREDs) or SiC Schottky Barrier Diodes (SBD) are often used. Alternatively, series-connected 600 V Si FREDs can be used. The boost switches Q1 to Q6 only need to block half the DC-link voltage, $U_{DC}/2$, which allows the selection of 650 V MOSFETs.

To achieve the PFC effect, the DC-link voltage needs to be boosted to a higher voltage than the rectified line voltage, for example, to U_{DC} = 750 V. The switch then needs to block $U_{DC}/2$ = 375 V. Keeping a margin of 25 %, a MOSFET with a breakdown voltage of $U_{DS,max} \geq 375/0.75 \geq 500$ V would be suitable. Consequently, two 650 V devices are suitable for DC-link voltages up to $U_{DC} \leq 975$ V keeping the 25 % margin into account. To achieve the output voltage required by the IEC61851-23 standard for DC-charging systems of 250 V ≤ U_{charge} ≤ 950 V, either the use of a transformer with a voltage-ratio, $U_{in}/U_{out} \geq 1$ in the DC-DC subcircuit or boosting the DC-link voltage to the required level is appropriate.

ISOPLUS Surface Mounted Power Device (SMPD) Package

The ISOPLUS Surface Mounted Power Device (SMPD) package combines the advantages of insulated power modules with surface mounted device (SMD) package technology. The SMD power package allows automatic assembly compared to through-hole technology (THT) devices as well as soldering in the same reflow process as other passive components. Therefore, process steps, and thus, cost can be reduced. The ISOPLUS SMPD package is based on a Direct Copper Bonding (DCB) ceramic substrate, which eases insulation coordination based on IEC 60664 and thermal management. The package is illustrated in Figure 3.

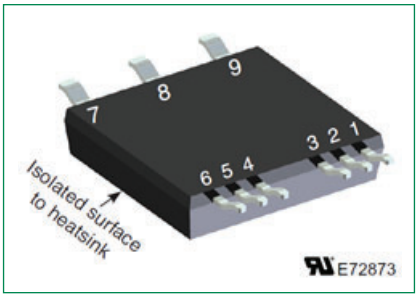

Figure 3. Rendering of the SMPD package, variant B, with three main terminals 7-9 and six auxiliary terminals 1-6

Due to the DCB substrate, different circuits can be integrated. The package covers a PCB footprint area of 25 × 32.7 mm² and has a height of 5.5 mm. The low weight of approximately 8.5 grams allows automatic assembly. The total DCB area is 21 × 23 mm² = 483 mm². Due to the lead frame, an area of approximately 330 mm² is available for die placing and bonding. Additionally, the lead frame provides a limited number of pins. The main terminals 7-9 can handle currents up to 100 A and terminals 1-6 up to 50 A each.

Fitting the 3-Level Vienna Rectifier into the ISOPLUS SMPD Package

The 3-level Vienna rectifier requires four power terminals and three gate drive terminals. To fit one phase-leg, as sketched in Figure 4, into the ISOPLUS SMPD package, the MOSFETs Q1 and Q2 need to be mounted in common-source configuration. The main current paths during positive and negative half-wave of the AC grid-voltage are indicated with red and blue arrows in Figure 4.

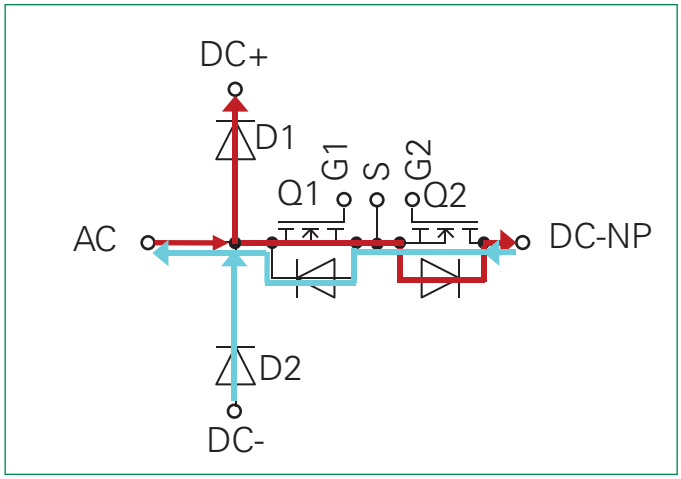

Figure 4. One phase-leg of the 3-level Vienna rectifier showing the current paths during positive (red) and negative (blue) half-wave of the AC grid-voltage

Consequently, the power terminals 7-9 of the ISOPLUS SMPD package can be used for the DC-link connection and three of the auxiliary terminals for the AC line connection. The resulting terminal configuration is sketched in Figure 5, which was previously presented in [3] as a concept.

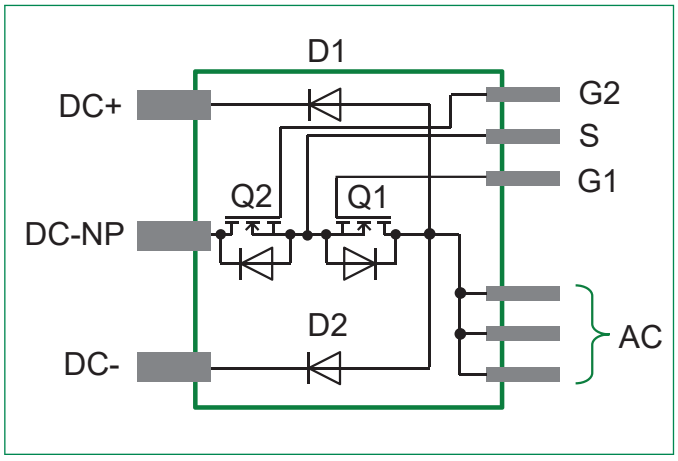

Figure 5. Circuit schematic of the 3-level Vienna rectifier phase-leg fit into the SMPD footprint

The terminal configuration was optimized to achieve the lowest possible stray inductances within the commutation loops, when considering the PCB layout. As the AC terminals are normally connected to a line inductor, compared to Figure 2, the stray inductance of this path is less critical than the commutation loop from the DC-neutral-point to the positive or negative DC-rail.

DCB Layout for the 3-Level Vienna Rectifier in ISOPLUS SMPD Package

Based on the terminal configuration and the results presented in [3], a DCB design was created, as sketched in Figure 6, excluding gate wire bonding

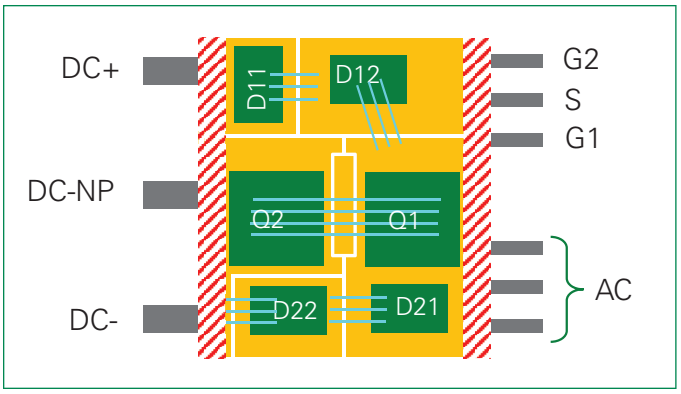

Figure 6. DCB layout concept for estimation if the available DCB area is sufficient for the maximum selected die sizes. Shaded areas indicate the placing of the lead frame.

The layout concept allows for other combinations of MOSFETs, and series-connected tandem diodes with lower blocking voltage. This helps to address different application-specific operating conditions or the use of SiC devices for higher switching frequencies.

First engineering samples of the 3-level Vienna rectifier were built based on the results in [3]. For the first batch, an IXFH22N65X2 MOSFET chip with a chip area of 25 mm² was selected [4]. On the Al_2O_3 DCB ceramic substrate, it achieved an approximate thermal resistance of $R_{th(j-c)}$ = 0.8 K/W. This would lead to a maximum drain-current of $I_{D,max}$ = 15 A at a junction temperature of T_{vj} = 150 °C and a given heatsink temperature of T_{HS} = 80 °C. Littelfuse diodes DSEP12-12A [5] rated for 1200 V, 12 A were utilized as D1 and D2.

Measurement Setup

In order to evaluate the switching performance of the 3-level Vienna rectifier prototype devices, double pulse tests were conducted. Therefore, a PCB was designed and manufactured to enable configuration of different test cases. The PCB is shown in Figure 7 and Figure 8.

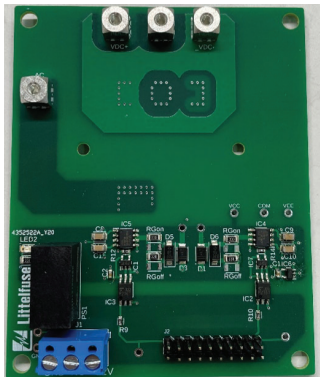

Figure 7. Top view of the test PCB having gate driver power supply, gate driver circuitry, and power connection terminal blocks

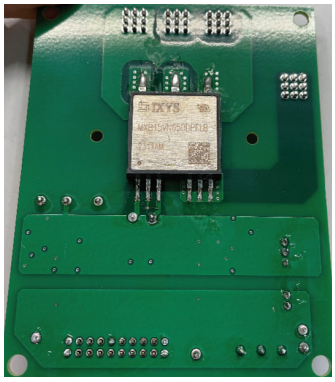

Figure 8. Bottom view of the test PCB holding the SMPD package with integrated 3-level Vienna rectifier

On the top side, the gate drive power supply and circuitry are assembled. For this test, a 9 A-rated Littelfuse gate driver IC IXD_609 was used and the possibility to employ separate gate resistances for turn-on and turn-off was implemented. The gate driver power supply was built using a DC-DC converter with output voltages of $U_{GS,on}$ = +15 V and $U_{GS,off}$ = -3 V. To connect the test board to the DC-link and the load inductor, screw terminal blocks are available.

Both MOSFET and diode combinations Q1+D1 and Q2+D2 were tested. For this, an air-cored coil of 330 µH was connected between the terminals DC+ and AC, as well as DC- and AC, respectively.

The test conditions and parameters for the double pulse testing are listed in Table 1. A wide range of test conditions using different gate resistance values from $R_{G,ext}$ = 6.7 Ω to $R_{G,ext}$ = 47 Ω were applied at different load currents from I_D = 10 A to I_D = 40 A.

Table 1. Test conditions for double pulse testing of the Vienna rectifier SMPD sample

Parameter	Symbol	Value
DC-link Voltage	U_{DC}	400 V
Gate Resistor	R_G	6.7…47 Ω
Drain Current	I_D	10…40 A
Gate Voltage	V_{GS}	-3/+15 V

The DC-link voltage for all test points was set to U_{DC} = 400 V. All tests were conducted at room temperature T_{amb} = 25 °C. Voltages were measured using Teledyne LeCroy HVD3106 high-voltage differential probes and the drain currents using a CWT Ultra-mini Rogowski coil.

From the measurements, it is also possible to calculate the stray inductances of the test setup during turn on of the MOSFETs Q1 and Q2, respectively, according to Equation (1).

$$L_\sigma = \Delta u/(di/dt) \qquad (1)$$

where Δu indicates the voltage drop of the drain-to-source voltage during the transient of the drain current di/dt of the MOSFET.

Measurement Results

The characterization of the first prototypes includes measurement of the stray inductances, static output characteristics, dynamic switching performance, and thermal resistance. The following section presents and discusses the measurement results.

Determination of Stray Inductances

From the measured waveforms in Figure 9 for the loop of Q1 & D1, the stray inductances of the PCB can be calculated according to Equations (2) and (3).

$$L_\sigma = 90\ V/(2.96\ A/ns) = 30\ nH \text{ for Q1 \& D1} \qquad (2)$$

$$L_\sigma = 70\ V/(3.08\ A/ns) = 23\ nH \text{ for Q2 \& D2} \qquad (3)$$

These are very low values, considering the DC-link connection via screw terminal blocks. The difference of the two stray inductances most likely originates from the internal DCB layout combined with the PCB layout.

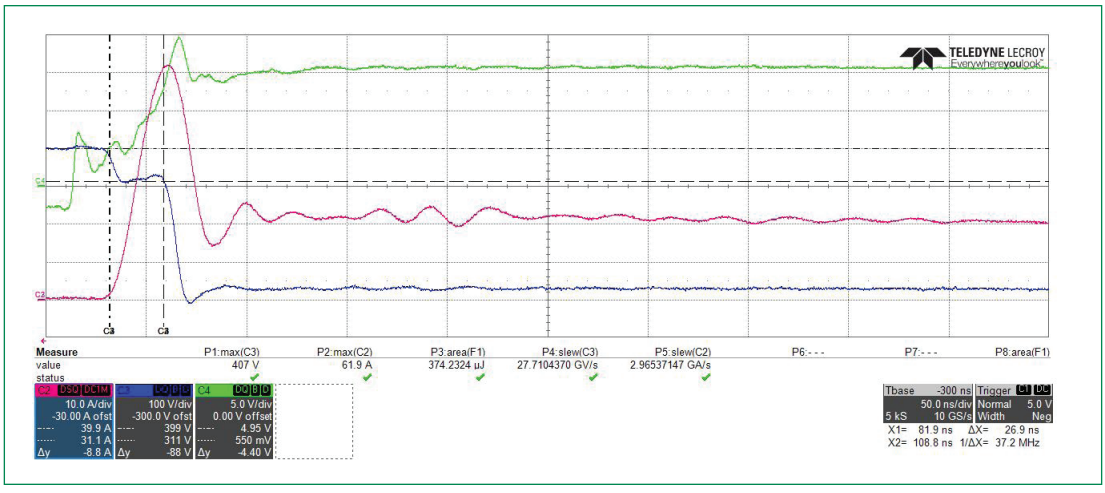

Figure 9. Turn-on waveforms of Q1 and D1 for determination of the stray inductance at U_{DC} = 400 V, I_D = 20 A, with C2 (red): i_D, C3 (blue): u_{DS}, C4 (green): u_{GS}

Static Device Characteristics

The static output characteristics of Q1 at a junction temperature of T_{vj} = 25 °C are represented in Figure 10 and at T_{vj} =125 °C in Figure 11.

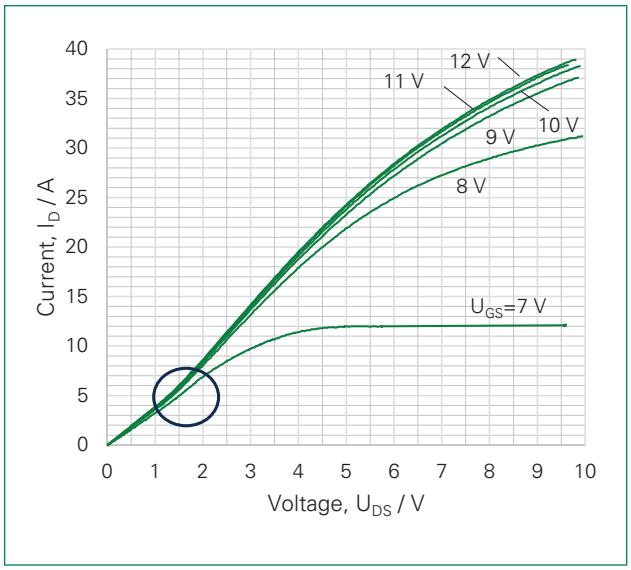

Figure 10. Static output characteristics of Q1, T_{vj} = 25 °C

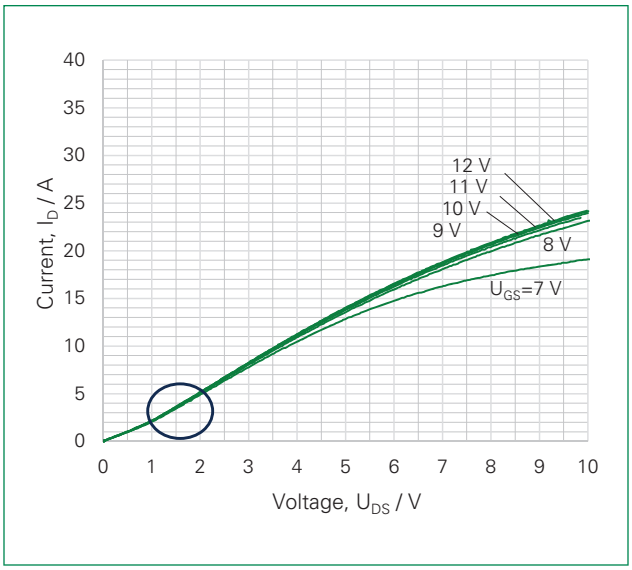

Figure 11. Static output characteristics of Q1, T_{vj} = 125 °C

Since the forward voltage is measured on both Q1 and Q2, the voltage includes the combined body diode voltage drop and channel resistance of Q2. This effect is represented by the inverting slope of the curve marked by the circles in Figure 10 and Figure 11. Additionally, it is possible to derive that the voltage U_{DS}, at which the slope changes, reduces with higher temperature from $U_{DS} \approx 1.3$ V at T_{vj} = 25 °C to $U_{DS} \approx 1.1$ V at T_{vj} = 125 °C. This originates from the negative temperature coefficient of the bipolar body diode of Q2. Furthermore, the conductivity modulation starts saturating at gate voltages $U_{GS} \geq 10$ V.

Switching Performance of the MOSFET

Besides the stray inductances of the setup and the static output characteristics, the dynamic double pulse test was utilized to determine the switching losses of the MOSFETs, as well as reverse recovery charge of the 1200 V diode in use. For this, both the combinations Q1-D1, as well as Q2-D2 were tested. The turn-off waveforms of Q1 at I_D = 40 A are depicted exemplarily in Figure 12 for a gate resistance of $R_{G,ext}$ = 47 Ω.

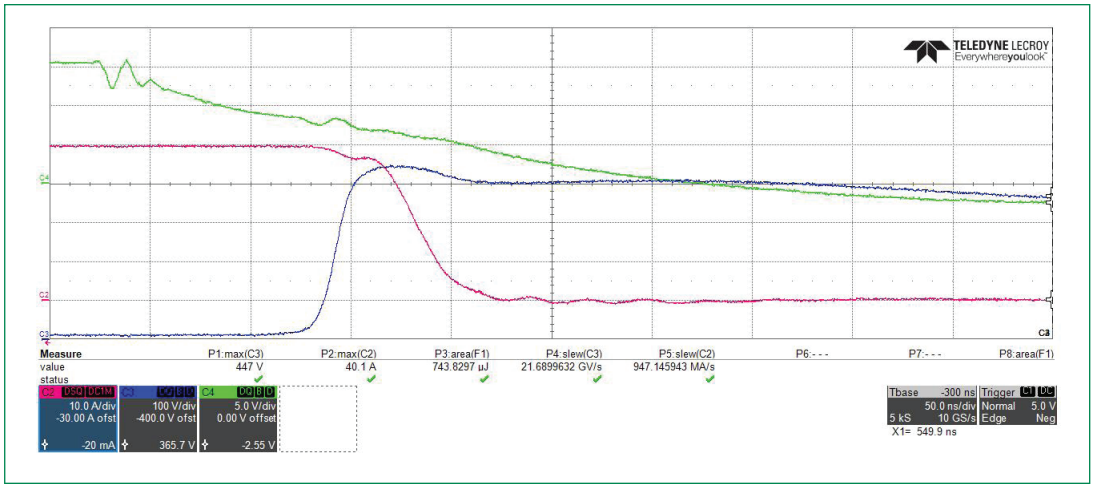

Figure 12. Turn-off switching waveforms of Q1 at I_D = 40 A and with $R_{G,ext}$ = 47 Ω. Green: u_{GS} (5 V/div), red: i_D (10 A/div), blue: u_{DS} (100 V/div)

The turn-on waveforms are illustrated in Figure 13 for the same test conditions.

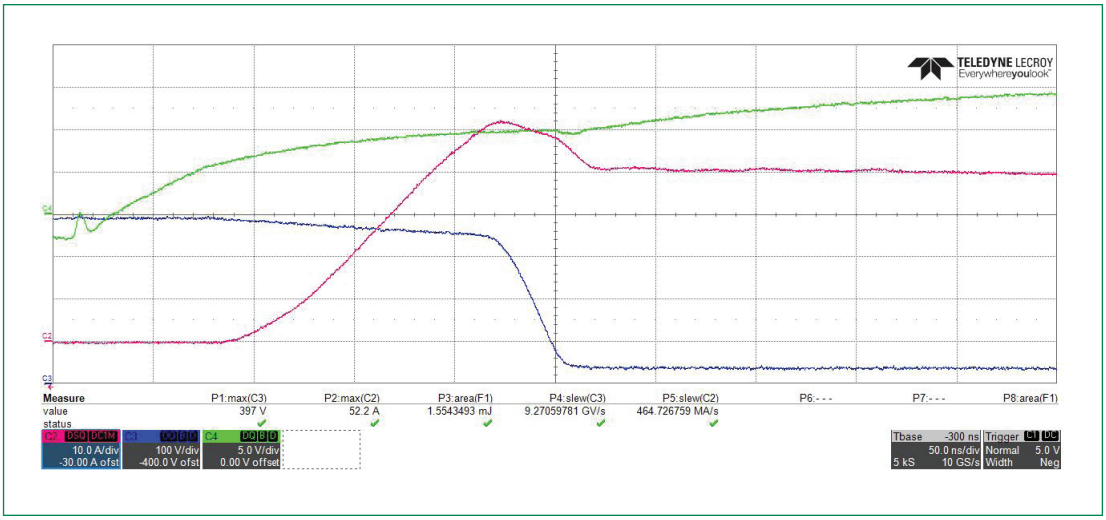

Figure 13. Turn-on switching waveforms of Q1 at I_D = 4 0 A and with $R_{G,ext}$ = 47 Ω. Green: u_{GS} (5 V/div), red: i_D (10 A/div), blue: u_{DS} (100 V/div)

With an external gate resistance of $R_{G,ext}$ = 47Ω, the switching losses are comparably high, namely E_{off} = 744 µJ and E_{on} = 1.55 mJ respectively. Therefore, the performance that can be achieved with lower external gate resistance is of interest. The resulting switching waveforms for $R_{G,ext}$ = 6.7 Ω are shown in Figure 14 for turn-off.

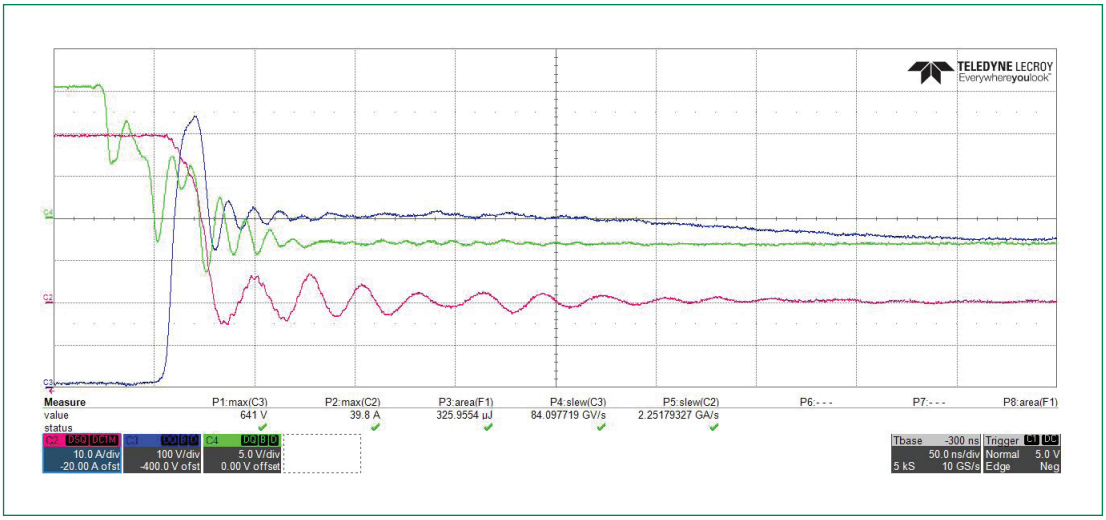

Figure 14. Turn-off switching waveforms of Q1 at I_D = 40 A and with $R_{G,ext}$ = 6.7 Ω. Green: u_{GS} (5 V/div), red: i_D (10 A/div), blue: u_{DS} (100 V/div)

The turn-on transition waveforms are illustrated in Figure 15 for the same test conditions.

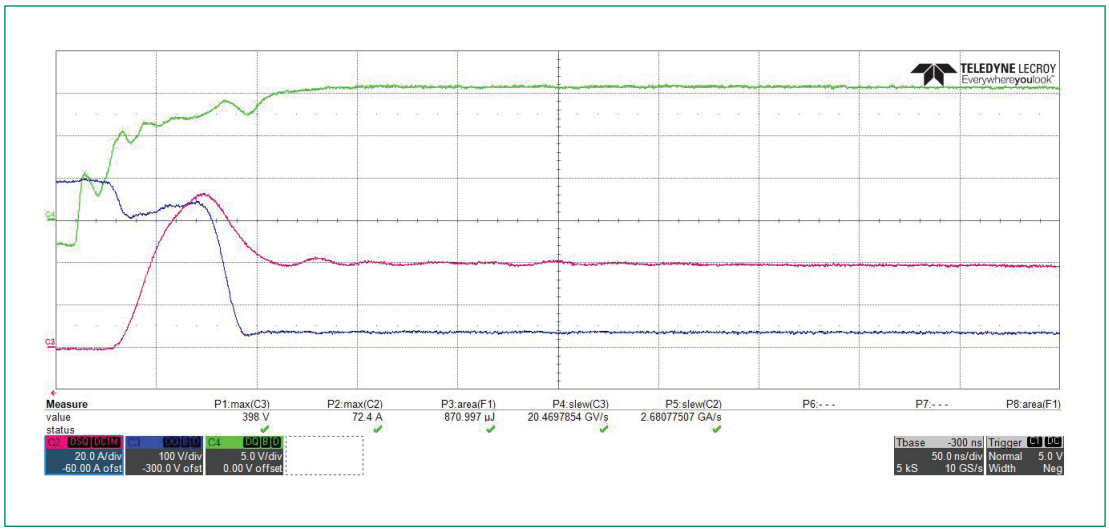

Figure 15. Turn-on switching waveforms of Q1 at ID = 40 A and $R_{G,ext}$ = 6.7 Ω. Green: u_{GS} (5 V/div), red: i_D (20 A/div), blue: u_{DS} (100 V/div)

The resulting switching losses are E_{off} = 326 µJ and E_{on} = 871 µJ respectively. The turn-off waveforms in Figure 14 reveal that some oscillations occurred and the high dv/dt caused some feedback to the gate voltage. However, it did not cause parasitic turn-on. On the other hand, the turn-on waveforms in Figure 15 do not show oscillations of the gate voltage.

Reverse Recovery of the Diode

The reverse recovery waveforms of the diode D1 at I_D = 40 A are depicted exemplarily in Figure 16 for a gate resistance of $R_{G,ext}$=47 Ω. The resulting di/dt is 0.49 kA/µs and the corresponding reverse recovery charge can be calculated to be E_{rec} = 111 µJ. The maximum reverse recovery current is I_{rrm} = 12 A.

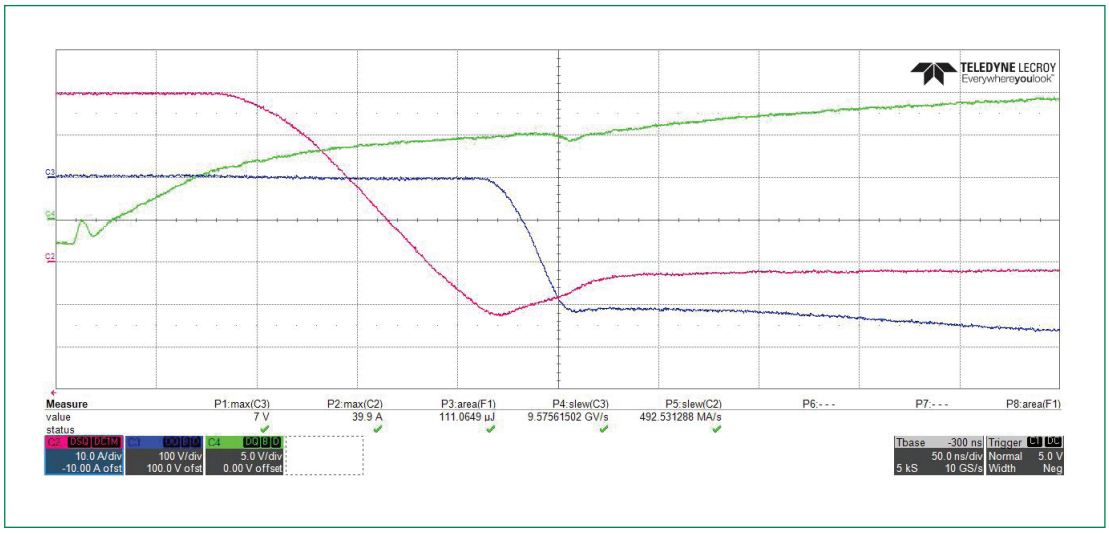

Figure 16. Diode reverse recovery waveforms for D1 at I_D = 40 A and with $R_{G,ext}$ = 47 Ω.Green: $u_{GS,Q1}$ (5 V/div), red: $i_{F,D1}$ (10 A/div), blue: $u_{R,D1}$ (100 V/div)

With lower gate resistance, the switching speed increases accordingly, as illustrated in Figure 17 when switching with $R_{G,ext}$ = 6.7 Ω. There, the reverse recovery charge reduces slightly to E_{rec} = 97 µJ at a di/dt = 2.3 kA/µs. However, the maximum reverse recovery current peaks to I_{rrm} = 16 A. Temperature dependance of reverse recovery was not investigated.

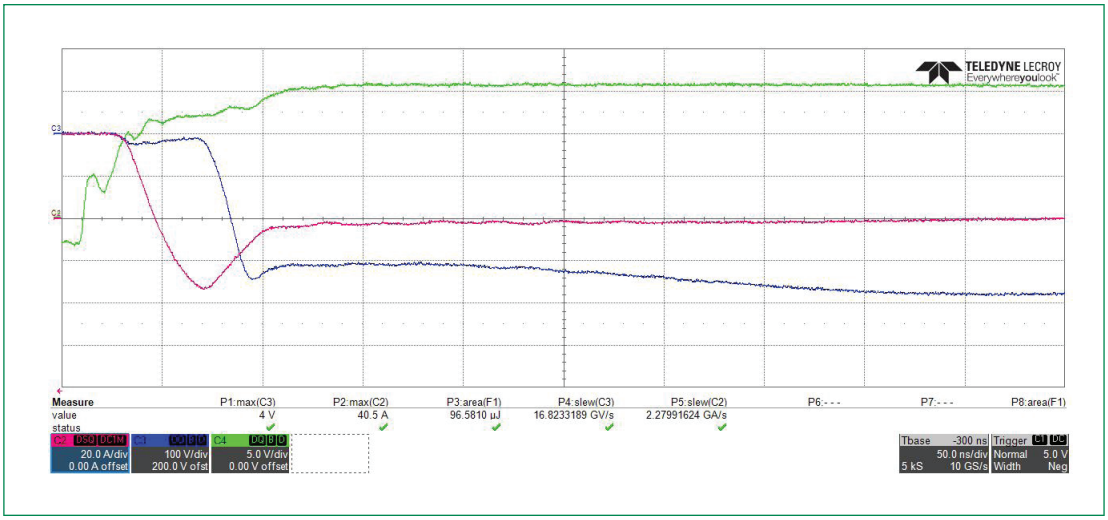

Figure 17. Diode reverse recovery waveforms for D1 at I_D = 40 A and with $R_{G,ext}$ = 6.7 Ω. Green: $u_{GS,Q1}$ (5 V/div), red: $i_{F,D1}$ (10 A/div), blue: $u_{R'D1}$ (100 V/div)

Switching Loss Comparison

The total switching losses of Q1 and D1 are illustrated in Figure 18. The measurements revealed only very slight differences between the combinations of Q1-D1 and Q2-D2, as illustrated in Figure 19 for $R_{G,ext}$ = 22 Ω. The deviations result from the PCB and DCB layout.

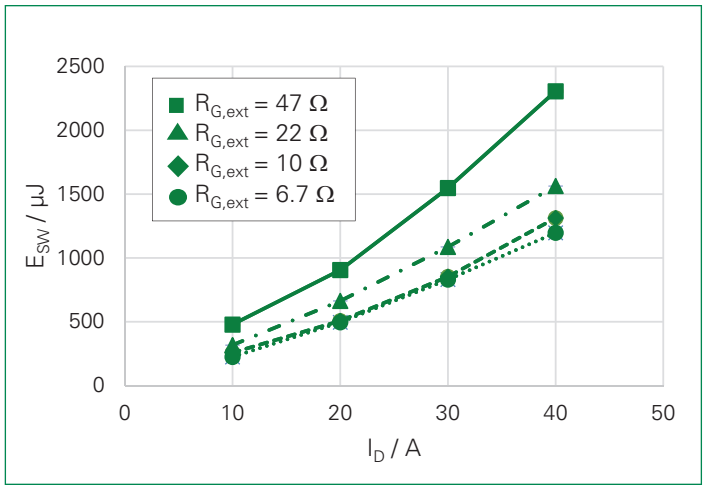

Figure 18. Switching loss energy E_{SW} of Q1

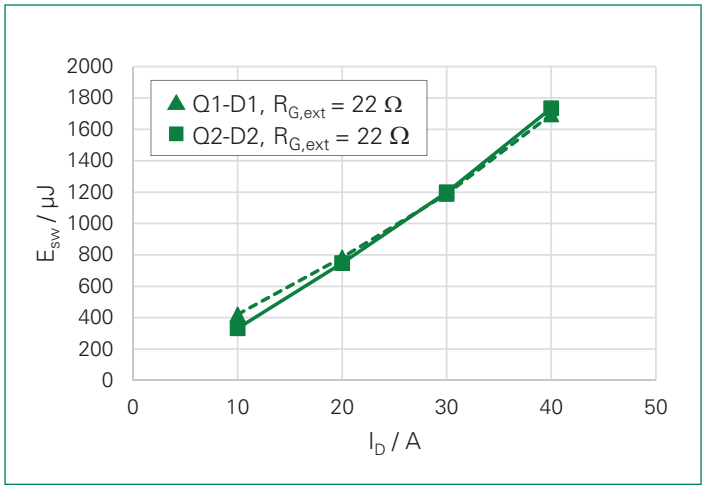

Figure 19. Comparison of total switching loss energy E_{SW} between Q1-D1and Q2-D2 combination, when using $R_{G,ext}$ = 22 Ω

Switching Speed Comparison

The switching speed curves, dv/dt and di/dt for Q1-D1, during turn-on are illustrated in Figure 20 and Figure 21, respectively.

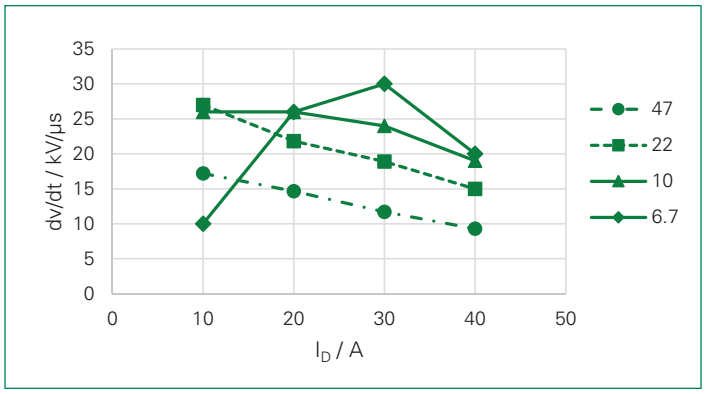

Figure 20. Turn-on switching speed dv/dt of Q1-D1 with different $R_{G,ext}$

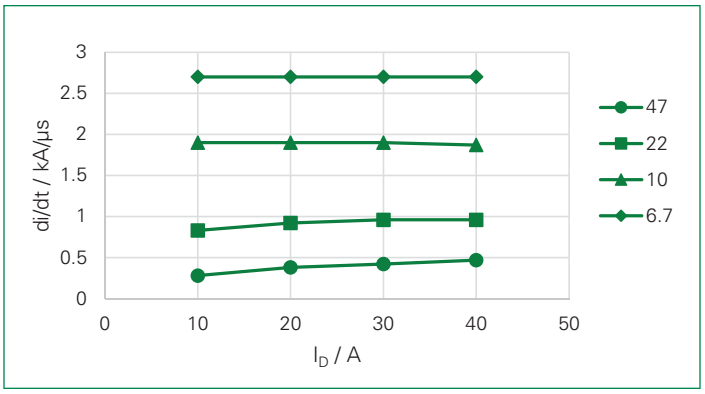

Figure 21. Turn-on switching speed di/dt of Q1-D1 with different $R_{G,ext}$

From the dv/dt values given in Figure 20, it can be concluded that the switching speed can be tuned with the external gate resistance as long as the value is selected in the range of $R_{G,ext}$ = 10…47 Ω. The same can be concluded for the current slope di/dt. Here, the difference from $R_{G,ext}$ = 6.7 Ω to 10 Ω is still significant. Since the dv/dt is not influenced at $R_{G,ext}$ = 6.7 Ω in a proportional way to di/dt, it can be concluded that the parasitic capacitances of the test setup and of the devices limit the dv/dt.

The switching speed curves dv/dt and di/dt for Q1-D1 during turn-off are illustrated in Figure 22 and Figure 23. From the dv/dt values given in Figure 20, it can be concluded that the switching speed can be tuned with the external gate resistance as long as the value is selected in the range of $R_{G,ext}$ = 10…47 Ω.

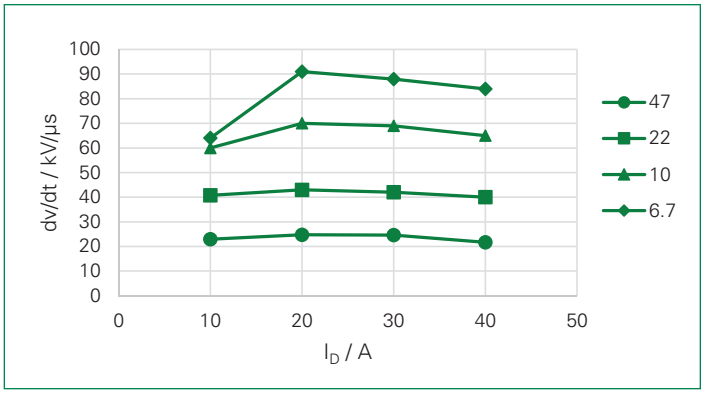

Figure 22. Turn-off switching speed dv/dt of Q1-D1 with different $R_{G,ext}$

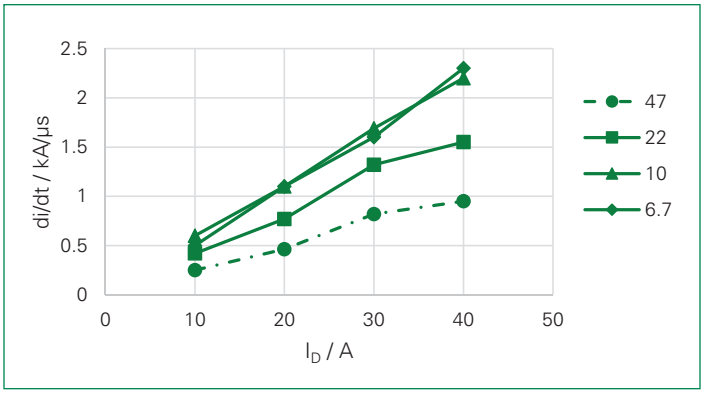

Figure 23. Turn-off switching speed di/dt of Q1-D1 with different $R_{G,ext}$

The turn-off waveforms exhibit contrary behavior with dependance on $R_{G,ext}$. From the dv/dt curves in Figure 22, it can be concluded that by fine-tuning $R_{G,ext}$, the voltage transient can be controlled. However, there is a limit to it at small drain currents due to the parasitic capacitances.

The current slope di/dt as shown in Figure 23 is controllable by the choice of gate resistance within the range of $R_{G,ext}$ = 10…47 Ω. There is no significant difference between $R_{G,ext}$ = 6.7 Ω and 10 Ω. The test results presented above can be used to support the application-specific design.

Thermal Performance of the 3-Level Vienna SMPD

The thermal resistance, $R_{th(j\text{-}h)}$, of each chip in the engineering samples was measured using a Littelfuse-specific test fixture. It was measured using a thermal grease thickness of 40 µm rolled on the backside of the SMPD package. This represents a practical approach used by customers and still leaves room for optimization. The results of $R_{th(j\text{-}h)}$ are listed in Table 2.

Table 2. Measured thermal resistance values of SMPD engineering sample

Device	Symbol	$R_{th(j\text{-}h)}$
Diode 1	D1	2.2 K/W
Diode 2	D2	2.1 K/W
MOSFET 1	Q1	1.0 K/W
MOSFET 2	Q2	1.0 K/W

The measured values match closely with the estimation given in [3].

Application-Specific Design

Based on the presented measurement results above, the application-specific losses can be estimated. The calculation method can be adopted from [3] and modified to the new target values. Hence, the target grid current will be I_{AC} = 16 A at an input voltage of U_{AC} = 400 V and switching frequency of f_{SW} = 48 kHz. The switching duty cycle as a function of the grid current is illustrated in Figure 24.

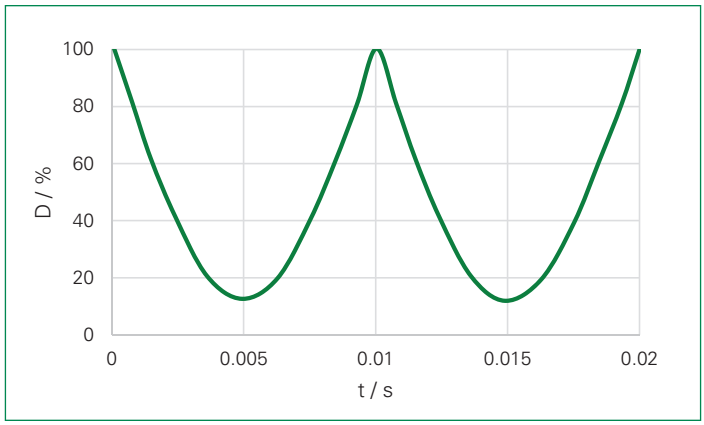

Figure 24. Duty cycle as a function of time for a DC-link voltage of U_{DC} = 750 V at a line voltage of $U_{AC,rms}$ = 400 V and an input current of I_{AC} = 16 A

The switching losses during the grid cycle can be linearized from the measured switching losses by the regression functions (4)-(6) for different gate resistances $R_{G,ext}$.

$$R_{G,ext} = 47\ \Omega: E_{SW}(i_D) = 0.825 \cdot i_D^2 + 19.99 \cdot i_D + 190.5 \quad (4)$$

$$R_{G,ext} = 22\ \Omega: E_{SW}(i_D) = 0.3275 \cdot i_D^2 + 25.195 \cdot i_D + 31.25 \quad (5)$$

$$R_{G,ext} = 10\ \Omega: E_{SW}(i_D) = 0.525 \cdot i_D^2 + 8.85 \cdot i_D + 117 \quad (6)$$

Based on these equations, the overall losses can be estimated as listed in Table 3. The values include the doubled switching losses of the MOSFET. At the target operating point in Table 3, total semiconductor losses of 145.8…156.9 W for the complete input stage can be expected. This results in a semiconductor efficiency of η = 98.6…98.7 %, which matches very well with the expected values in [3].

Table 3. Calculated semiconductor losses of the SMPD prototype in a Vienna PFC at f_{SW} = 48 kHz and input current of I_{AC} = 16 A at T_{vj} = 125 °C

Parameter	@R_G = 10 Ω	@R_G = 22 Ω	@R_G = 47 Ω
Switching losses per MOSFET	4.6 W	5.8 W	**8.3 W**
Conduction losses per MOSFET	22.3 W		
Conduction losses per MOS Bodydiode	3.5 W		
Conduction losses per Diode D1 and D2	18.2 W		

The resulting increase of the junction temperatures ΔT_{vj} can be estimated as given in Table 4, based on the given thermal resistances of the chips in Table 2. Consequently, a heatsink temperature of T_{HS} = 80 °C will keep the power semiconductors below their thermal limits at these targeted operating conditions.

Table 4. Increase of junction temperatures for the given losses of Table 3 for $R_{G,ext}$ = 47 Ω

Device	$R_{th(j-h)}$	ΔT_{vj}
Diode 1	2.2 K/W	40.0 K
Diode 2	2.1 K/W	38.2 K
MOSFET 1	1.0 K/W	34.1 K
MOSFET 2	1.0 K/W	34.1 K

Summary

In this article, the design proposal for fitting a Vienna rectifier phase-leg into the Littelfuse ISOPLUS SMPD package is presented and evaluated. The article presents the concept of the prototype DCB layout as well as the background of the pin layout for stray inductance optimization. Additionally, a test setup to conduct dynamic characterization of the SMPD samples with integrated Littelfuse ultrajunction silicon MOSFET IXFH22N65X2 and Littelfuse DSEP12-12A silicon FRED is presented. The thorough analysis of dynamic switching performance as well as static characterization provides a good basis to further extend the product range. The application-related design process to estimate losses in a practical approach showcases that the presented solution perfectly combines the cost-effective silicon-based technology with high efficiency, without the ultimate need for wide band-gap devices. It might be obvious that SiC or GaN devices will dissipate lower losses. However, depending on the target operating conditions, highest efficiency is not always the highest priority. For design engineers, system designers, and for keeping a stable supply chain, a full silicon solution is still worth consideration, especially in trending topics such as the EV-charging infrastructure or other systems connected to the public grid.

References

[1] Hypercharger by alpitronic, https://www.hypercharger.it/hyc400/, accessed on 2023-10-17
[2] ABB Terra 360 HPC, https://new.abb.com/ev-charging/terra-360, accessed on 2023-10-17
[3] Haehre et. al., Evaluation of Silicon-Based 3-Level T-Type Neutral Boost Rectifier Integrated into SMPD Package for EV-Charger Application, PCIM Europe 2023 conference, Nuremberg, Germany
[4] Littelfuse IXFH22N65X2, https://www.littelfuse.com/assetdocs/littelfuse-discrete-mosfets-ixf-22n65x2-datasheet?assetguid=e2d277e7-bb4f-4961-8db0-9c5942153fd5, accessed on 2023-10-17
[5] Littelfuse DSEP12-12A, https://www.littelfuse.com/assetdocs/littelfuse-power-semiconductors-dsep12-12a-datasheet?assetguid=afbcc1ff-023d-4f05-945c-a5bdf624e7b8, accessed on 2023-10-17